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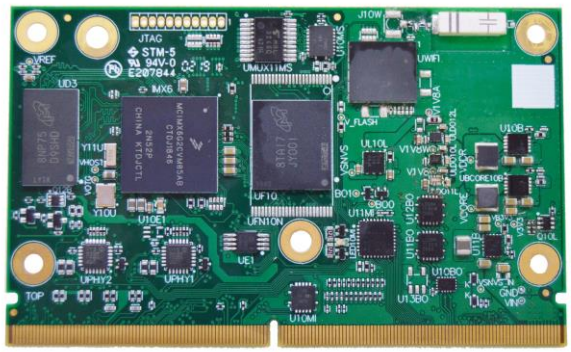

IGEP™ SMARC iMX6-UL/ULL

HARDWARE REFERENCE MANUAL

SMARC module

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

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1 USER INFORMATION

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2 INTRODUCTION

2.1 PRODUCT DESCRIPTION

The IGEP™ SMARC iMX6-UL and IGEP™ SMARC iMX6-ULL are industrial ultra-low computers based on iMX6 processor family by NXP, featuring single ARM Cortex-A7 core, which operates at speeds of up to 528 MHz and 792 MHz respectively.

It's an industrial computer module (it can work in a temperature range from -40ºC to +85ºC), in a very low profile according the standard form factor SMARC by SGET (its size is only 82,00 mm x 50,00 mm).

For development purposes there is also available an expansion board (IGEP™ SMARC EXPANSION) to complete the module. It can be used as the fastest way to develop the user's final application before the prototyping phase. This expansion board can be used with all IGEP™ SMARC modules.

Highlights:

- Fully tested, highly reliable, scalable, efficient and high performing board that allows customers to focus on their end application.
- Designed for industrial range purposes (temperature range: -40ºC to +85ºC).
- Form factor according to small size SMARC (82,00 mm x 50,00 mm).
- Easy connectivity through MXM3 graphic cards type connector: 314-pin, 0,5 pitch right angle.
- 1V8 I/O level digital signals.
- JTAG interface available.
- Based on NXP iMX6-UL or iMX6-ULL processor, both with simple ARM Cortex-A7 core.
- Two available 10/100 Mbps Ethernet MAC+PHY interface.
- Flexible Flash Memory combinations (customized option).
- WiFi 802.11 b/g/n / Bluetooth 4.2 connectivity
- RAM memory size: Up to 1 GB.
- Flash memory size: Up to 64 GB eMMC.
- Low Power solution.
- Compatible with SMARC modules.

2.2 IGEP™ SMARC iMX6-UL/ULL BENEFITS AND APPLICATIONS

There are a lot of advantages that developers will find in the IGEP™ SMARC iMX6-UL/ULL series, reducing the implementation time and saving costs on their designs. Amongst others, the main benefits are the following:

- Easy scalability between different modules (even with other processors) thanks to the SMARC standard.
- Compact and powerful core for new products.
- Robust and easy to mount due to the MXM3 314-pin connector.
- Reduced time to market.
- Low power consumption ≤ 2W.

- Industrial Temperature Range -40 to +85ºC.
- Extended life range product.

At the same time, it can be implemented for all kind of end applications. Here there are just a few ones, although the list can be as long as the imagination.

- Connected vending machines.
- Home / Building automation (IoT applications).
- Human Interface.
- Industrial Control.
- Test and Measurement.
- Artificial Intelligence

2.3 SMARC STANDARD

The IGEP™ SMARC iMX6-UL/ULL accomplish the SMARC 1.1 standard with some components of SMARC 2.0 version, which is defined by SGET.

The SMARC ("Smart Mobility Architecture") is a computer Module definition targeting applications that require low power, low costs, and high performance. This standard is based on ULP-COM (Ultra Low Power Computer-on-Modules). The Modules will typically use ARM SoCs (System on Chip) families or similar.

Two Module sizes are defined: 82mm x 50mm **(**IGEP™ SMARC iMX6-UL/ULL**)** and 82mm x 80mm. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin (156 on TOP side and 158 on BOTTOM side) right angle connector (the connector is sometimes identified as a 321-pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

2.4 SMARC FORM FACTOR FEATURE SUMMARY

Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.

- Two Module sizes:
  - 82mm x 50mm
  - 82mm x 80mm
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards.
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out.
  - Multiple sources for Carrier Board connector
  - Low cost
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom)
    - Other stack height options available, including 2.7mm, 5mm, 8mm

        - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm
    - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
    - Robust, vibration resistant connector.
- Module input voltage range: 3.0V to 5.25V
    - Allows operation from 3.6V nominal Lithium-ion battery packs.
    - Allows operation from 3.3V fixed DC supply.
    - Allows operation from 5.0V fixed DC supply.
    - Single supply (no separate standby voltage).
    - Module power pins allow 5A max.
- Low power designs
    - Fanless
    - Passive cooling
    - Low standby power
    - Design for battery operation
    - 1.8V default I/O voltage

2.5 IGEP™ SMARC iMX6-UL/ULL SERIES

The SMARC iMX6-UL/ULL series are composed by two models, with different processor. Both include WiFi 802.11 b/g/n / Bluetooth 4.2 connectivity.

The SMARC iMX6-UL model is composed by an industrial iMX6-UL processor at speed 528 MHz, the other model SMARC iMX6-ULL is composed by an industrial iMX6-ULL processor at speed up to 792 MHz.

Other combinations are available. Contact with IATEC's Sales Department for other configurations.

2.6 PARTS NUMBERS

Depending on the module configuration, the module has different parts numbers.

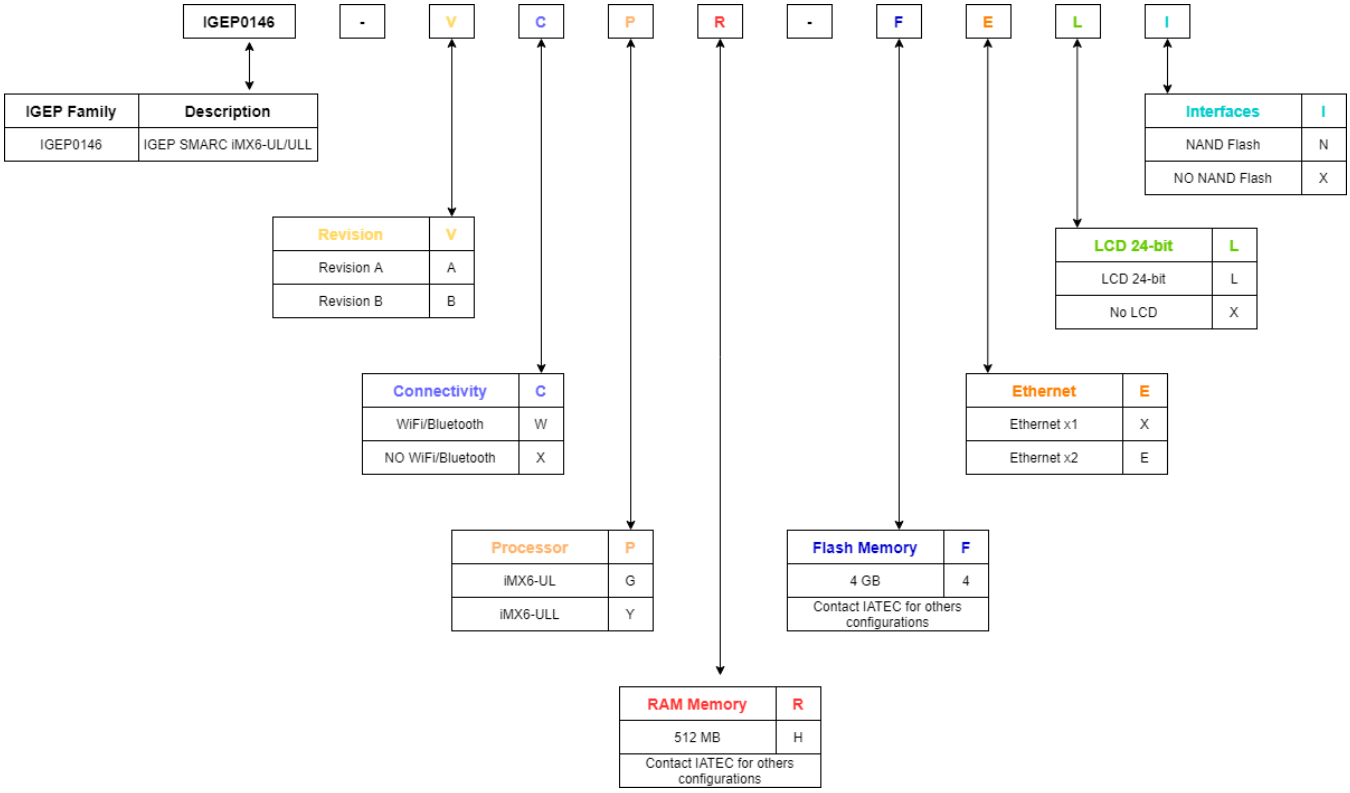

Figure 1 IGEP™ SMARC iMX6-UL/ULL Possible Part Number

Part Number	IGEP™ Device	Description
IGEP0146-BWGH-4ELX	SMARC iMX6-UL WiFi	Processor: iMX6-UL RAM Memory: 512 MB Flash Memory: 4 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 Ethernet x 2 LCD 24-bit
IGEP0146-BXGH-4XXX	SMARC iMX6-UL No WiFi	Processor: iMX6-UL RAM Memory: 512 MB Flash Memory: 4 GB Ethernet x 1
IGEP0146-BWYH-4ELX	SMARC iMX6-ULL WiFi	Processor: iMX6-ULL RAM Memory: 512 MB Flash Memory: 4 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 Ethernet x 2 LCD 24-bit
IGEP0146-BWGH-4ELN	SMARC iMX6-UL WiFi	Processor: iMX6-UL RAM Memory: 512 MB Flash Memory: 4 GB NAND flash Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2 Ethernet x 2 LCD 24-bit

Table 1 IGEP™ SMARC iMX6-UL/ULL Ordering Information.

3 HARWARE OVERVIEW

3.1 IGEPTM SMARC iMX6-UL/ULL

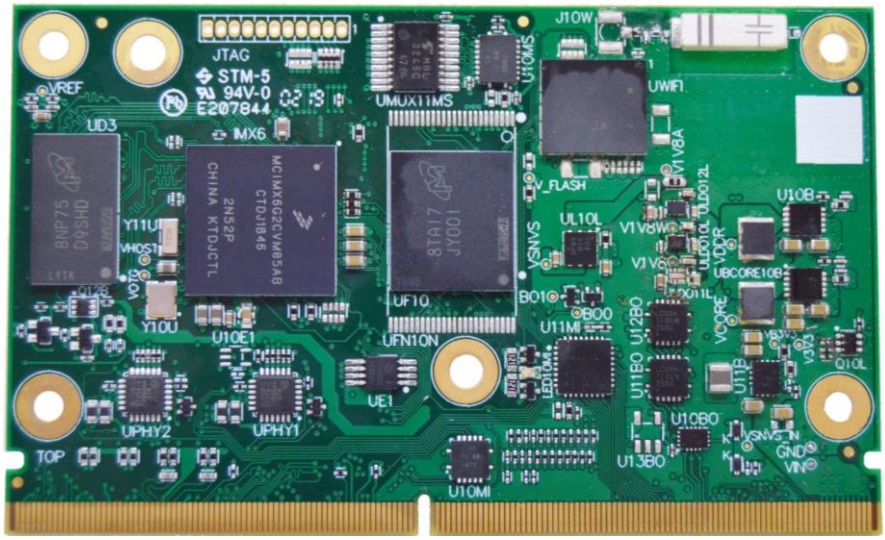

Figure 2 SMARC iMX6-UL/ULL – Top View

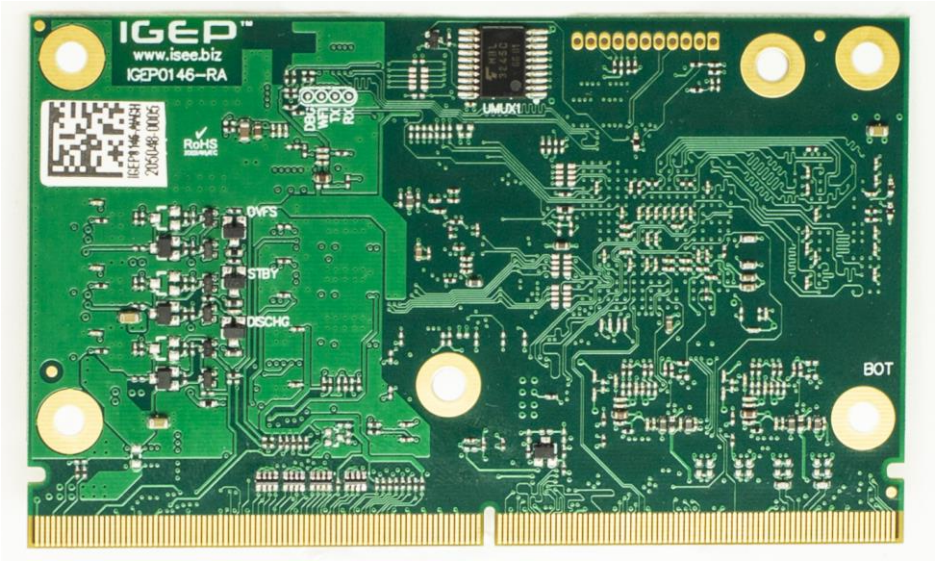

Figure 3 SMARC iMX6-UL/ULL – Bottom View

3.2 IGEP™ SMARC iMX6-UL/ULL BLOCK DIAGRAM

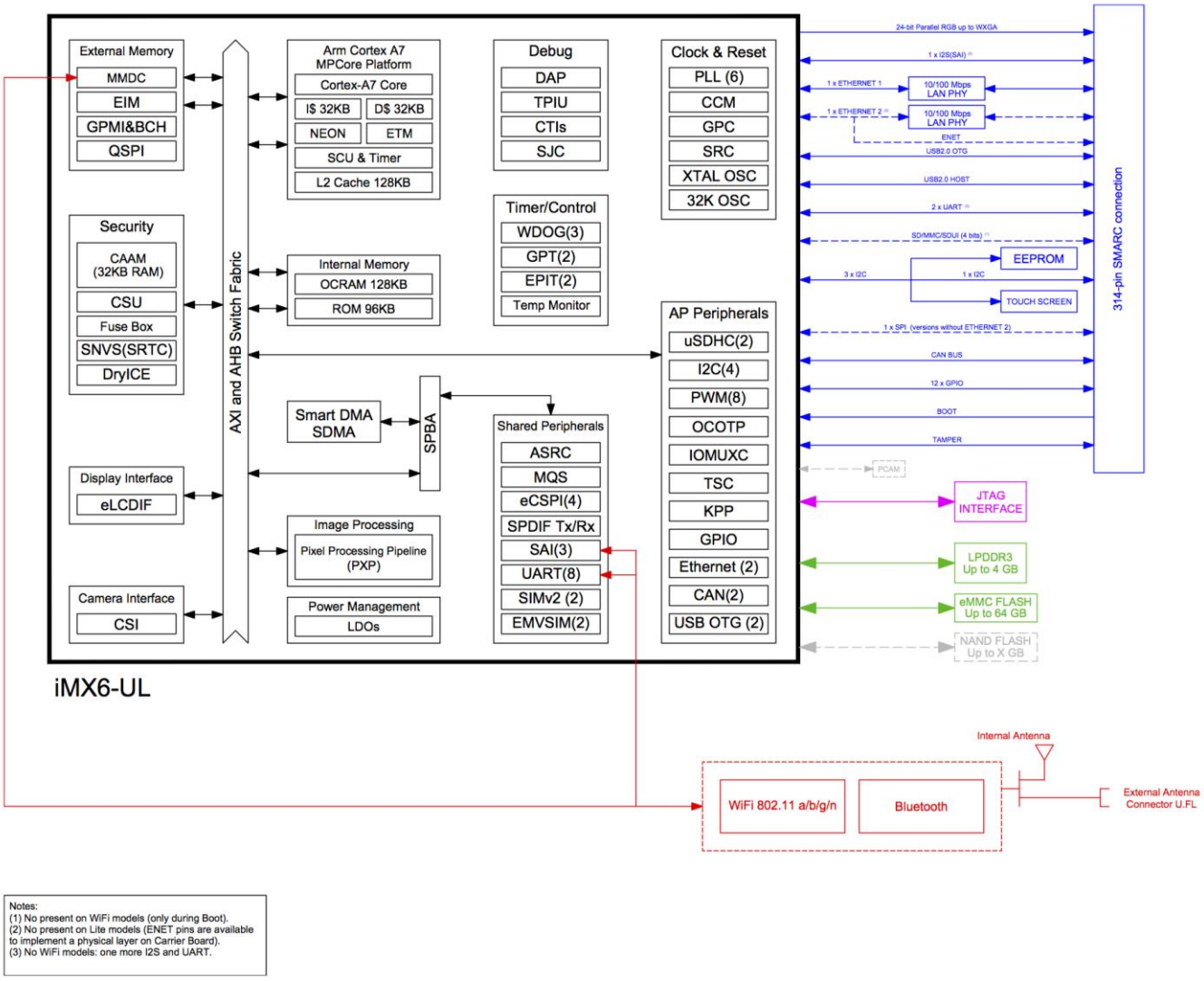

Figure 4 IGEP™ SMARC iMX6-UL Block Diagram

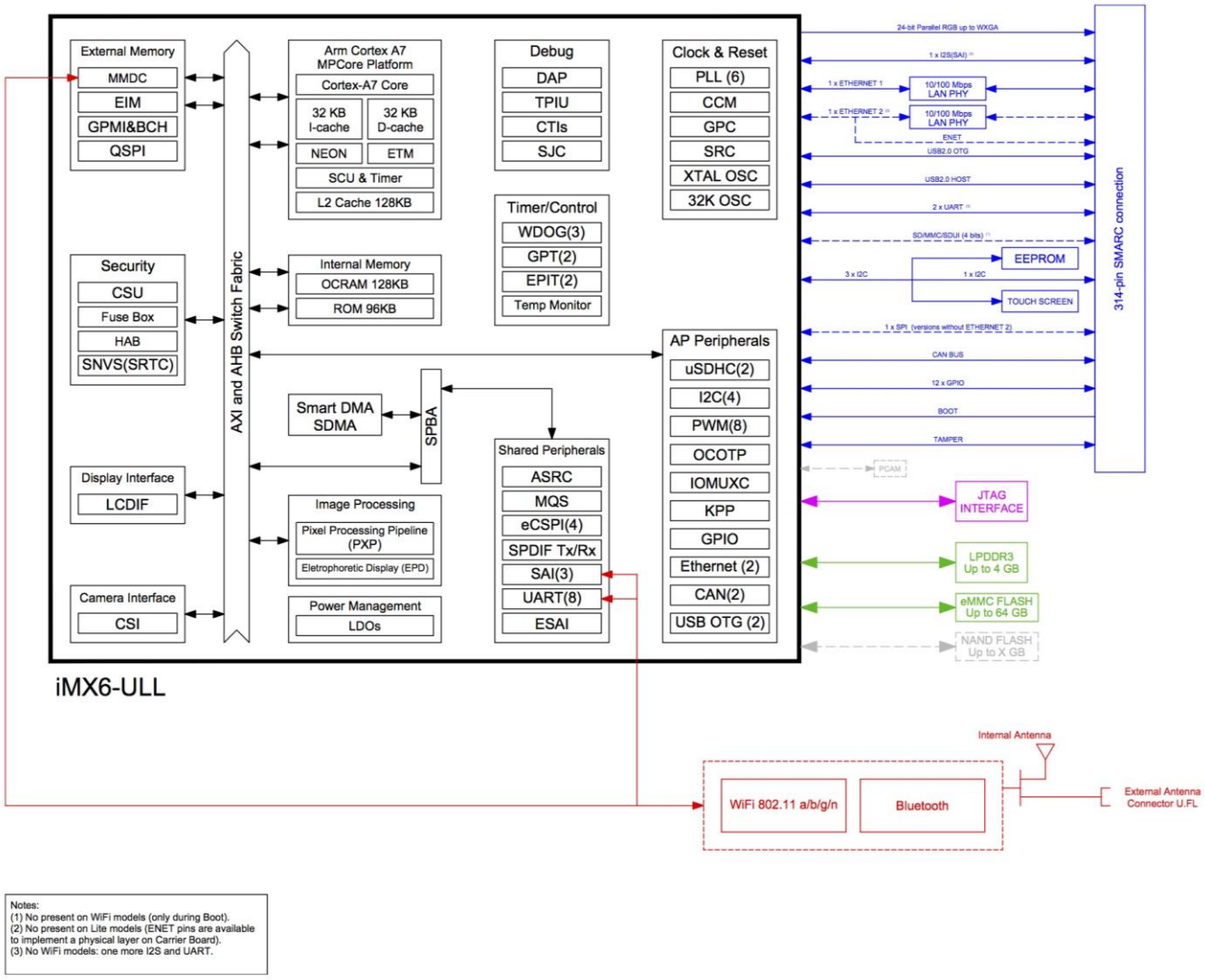

Figure 5 IGEP™ SMARC iMX6-ULL Block Diagram

3.3 IGEP™ SMARC iMX6-UL/ULL FEATURES

Feature	Specifications
Processor	NXP iMX6 UltraLite/UltraLite Lite CPU: ARM Cortex-A7 NEON SIMD Coprocessor Frequency: 528 MHz (up to 792 MHz in ULL version)
Memory	RAM: Up to 1 GB LPDDR3 Flash: Up to 64 GB eMMC EEPROM: Serial I2C 32 Kb
Camera Interface	1 x Parallel Camera up to 24-bit and 148.5MHz pixel clock Support BT.656 interface
Display	1 x 24-bit Parallel RGB up to WXGA (1366x768) at 60 Hz Support: 24-bit, 18-bit, 16-bit and 8-bit parallel display
Digital Audio	1 x I2S(SAI) (No WiFi versions: 2x, shared with JTAG)
Network	Up 2 Ethernet: 10/100 Mbps WiFi: Certified 802.11 b/g/n (Access Point: Yes) Bluetooth: 4.2
Antenna	Internal WiFi/Bluetooth antenna Optional: U.FL connector for external antenna
USB	1 x USB 2.0 OTG (with integrated phy) 1 x USB 2.0 Host (with integrated phy)
External Interfaces	2 x UART (No WiFi versions: 3x) 2 x I2C 1 x SPI (without Ethernet 2) 1 x CAN 12 x GPIO 1 x JTAG 2 x 12-bit ADC
OS Support	Linux Kernel 4.9 Distributions: Ubuntu 16.04, Yocto 2.3, Debian
Power Supply	Power from expansion connectors: From 3,0 V to 5,25 V Digital I/O voltage: 1,8 V
Power Consumption	0.27 A
Thermal	Industrial temperature: -40ºC to +80ºC
Form Factor	Small SMARC size: 82,00 mm x 50,00 mm
Humidity	93% relative Humidity at 40 ºC, non-condensing (according to IEC 60068-2-78)
MTBF	131400 hours (>15 years)

Table 2 On-board features

3.4 IGEP™ SMARC iMX6-UL/ULL COMPONENTS MAP

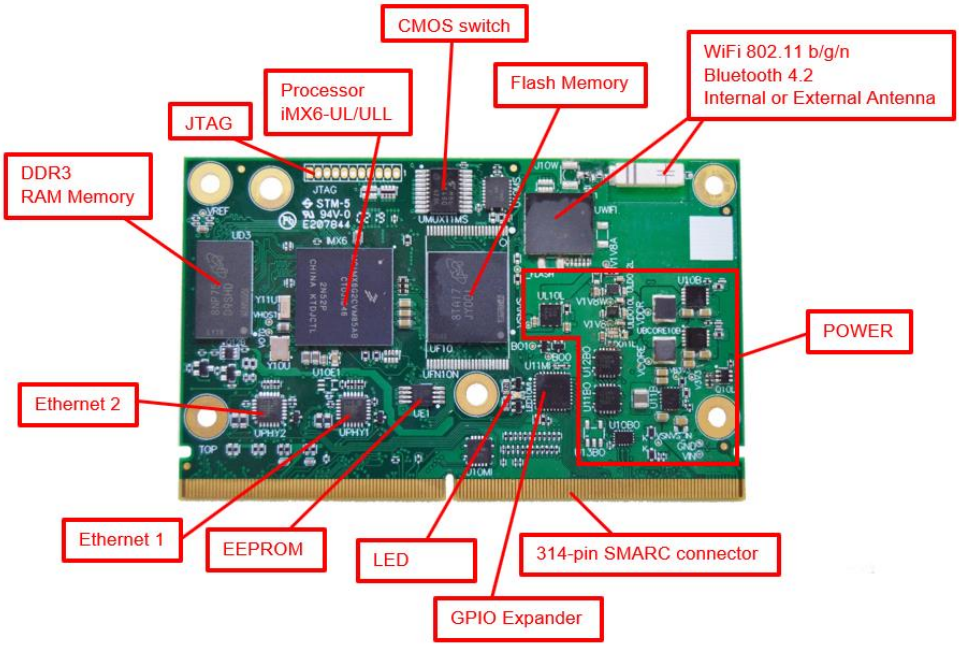

Figure 6 SMARC iMX6-UL/ULL Components Map

3.5 NXP iMX6-UL/ULL PROCESSORS

The iMX6-UL by NXP is a highly integrated processor based on the ARM Cortex-A7 with a frequency speed of 528 MHz (Industrial version).

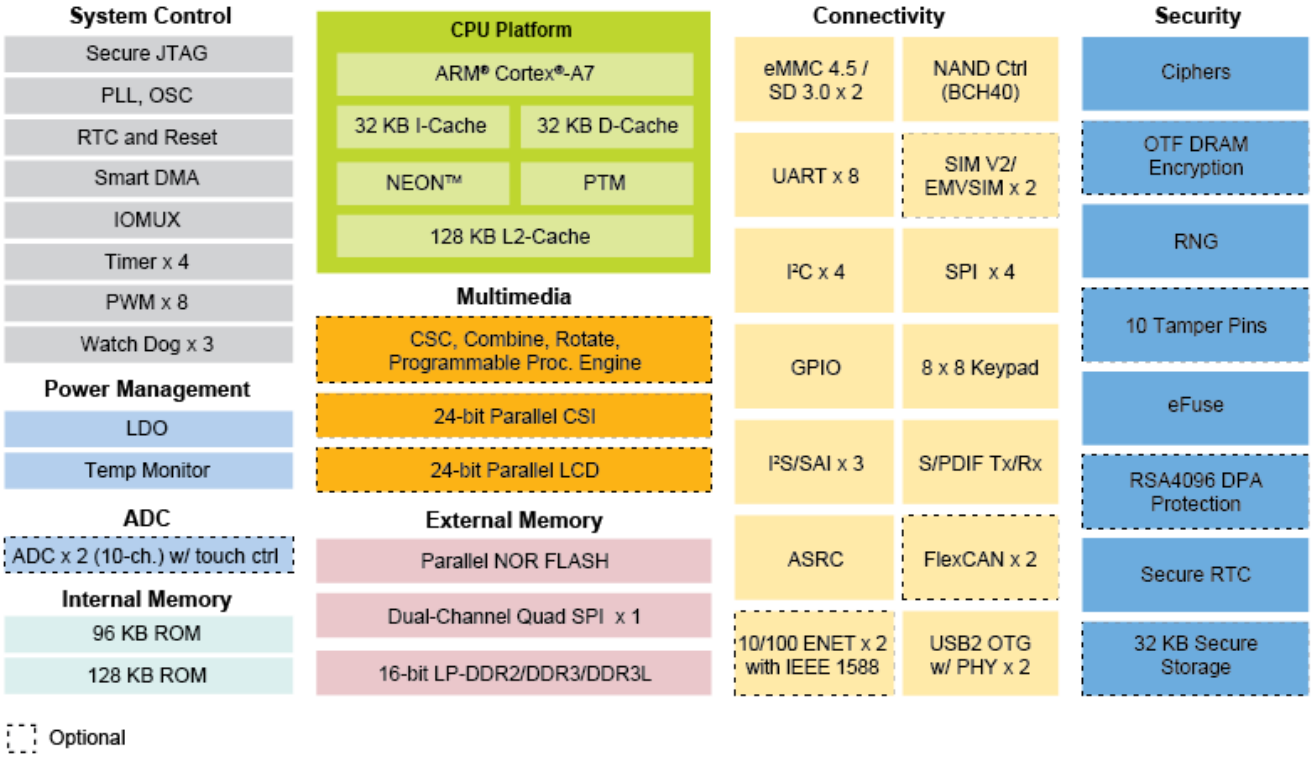

Figure 7 NXP iMX6-UL Processors Block Diagram

The iMX6-ULL by NXP is a highly integrated processor based on the ARM Cortex-A7 with a frequency speed of 792 MHz (Industrial version).

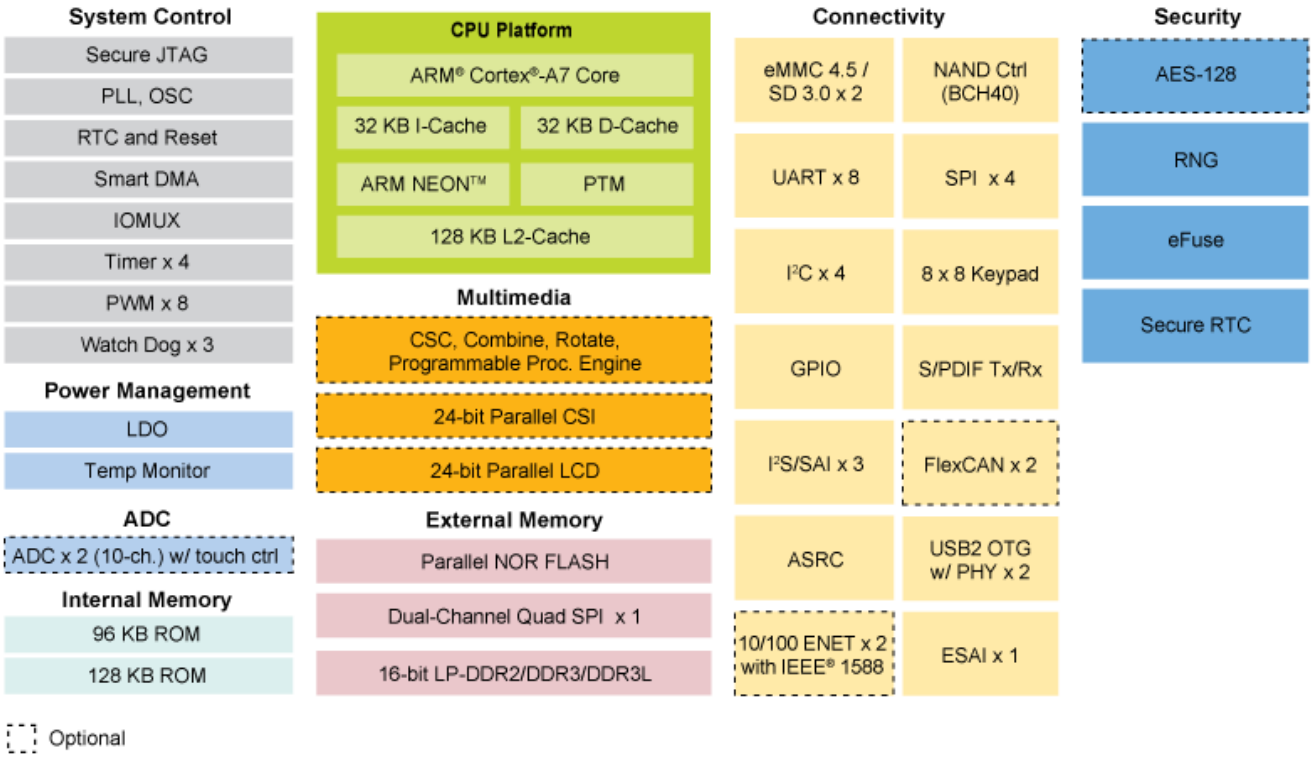

Figure 8 NXP iMX6-ULL Processors Block Diagram

4 SMARC EXPANSION CONNECTOR INTERFACE

4.1 SMARC INTERFACE DEFINITION

IGEP™ SMARC iMX6-UL/ULL has a 314-pin SMARC interface (156 on TOP side and 158 on BOTTOM side), providing source power and 1V8 CMOS signals to support lots of iMX6-UL/ULL processor features which could be used in custom application. The module sizes are 82mm x 50mm as the SMARC standard defines.

Next figure shows the area and pin numbering of the SMARC interface.

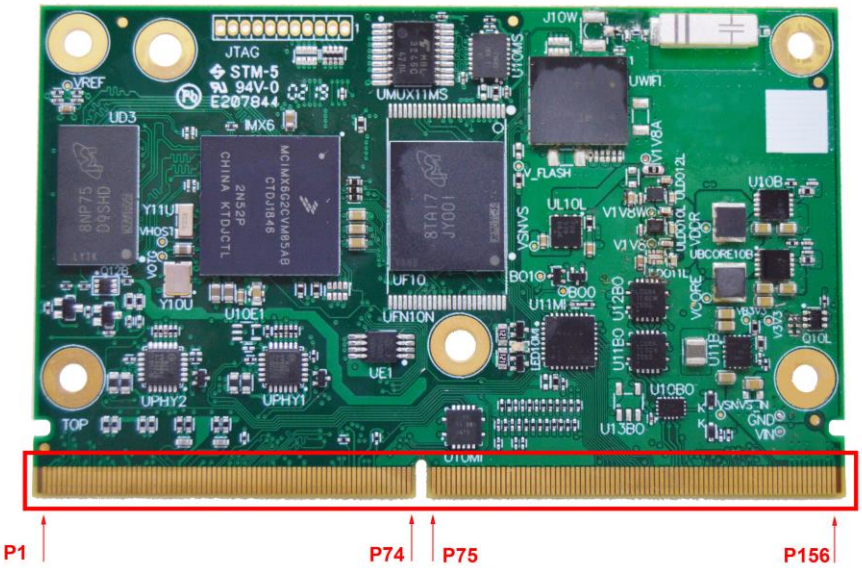

Figure 9 SMARC interface area (TOP Side)

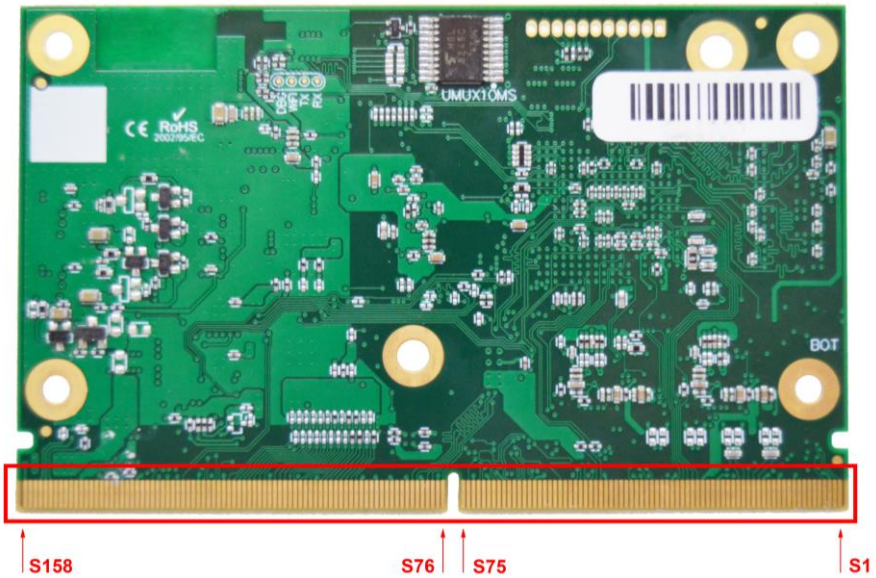

Figure 10 SMARC interface area (BOTTOM Side)

The IGEP™ SMARC iMX6-UL/ULL modules can be inserted like a target through this SMARC interface to any of the standard connectors existing on the market. Next table shows some valid references (consult the page 73 on the SMARC 2.1 Specification to find more information).

Manufacturer	Part Number	Height
FOXCONN	AS0B821-S43B-*H	4,3 mm
FOXCONN	AS0B821-S43N-*H	4,3 mm
FOXCONN	AS0B826-S43B-*H	4,3 mm
FOXCONN	AS0B826-S43N-*H	4,3 mm
JAE	MM70-314B2-1-R500	4,3 mm
Aces	91781-314 2 8-001	5,2 mm
FOXCONN	AS0B821-S55B-*H	5,50 mm
FOXCONN	AS0B821-S55N-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B821-S78B-*H	7,80 mm
FOXCONN	AS0B821-S78N-*H	7,80 mm
FOXCONN	AS0B826-S78B-*H	7,80 mm
FOXCONN	AS0B826-S78N-*H	7,80 mm
Yamaichi	CN113-314-2001	7,80 mm

Table 3 Valid SMARC connector part numbers

Developers must consider the SMARC connector height according to their expansion board needs.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards.

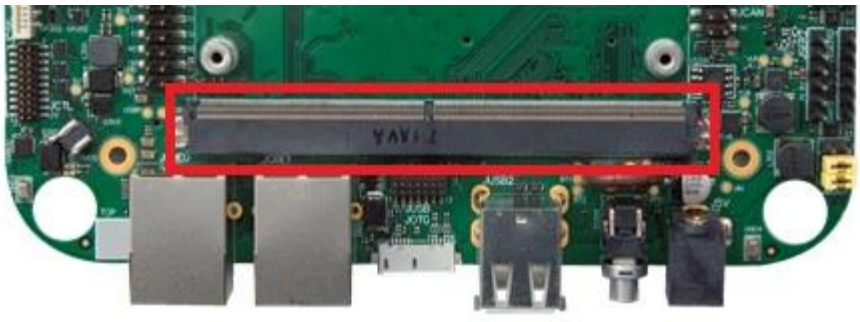

Figure 11 SMARC CONNECTOR

4.2 PINOUT TABLE OF SMARC (VERSION) EXPANSION INTERFACE

This chapter contains all the pinout details for the SMARC-314 expansion interface. The table below shows the meaning of each column in table 5, where is collected all the pins and its main functions.

COLUMN	INFORMATION PROVIDED	
PIN	Indicates the pin number of the SMARC interface. It is either for Primary Side (Top Side, P#) and Secondary Side (Bottom Side, S#)	
VOLTAGE LEVEL	Signal Level Voltage	
	3V to 5V25	3V to 5V25 signal
	3V3	3,3 V signal
	1V8	1,8 V signal
	PHY MDI	Differential analog signaling for PHY Media Dependent Interface.
	LVDS D-PHY	LVDS signaling used for MIPI CSI camera interfaces.
	TMDS	LVDS signaling used for HDMI display interfaces.
	USB	DC coupled differential signaling used for traditional (non-Super-Speed) USB signals
	USB SS	LVDS signaling used for Super Speed USB 3.0
	GND	Digital ground.
	NC	No connected. This pin should be floating.
TYPE	Indicates pin type.	
	Power	Power signal.
	Input	CMOS input pin.
	Output	CMOS output pin.
	IO	CMOS input and output pin.
	Output OD	Open drain output pin.
	I/O OD	Open drain input and output pin.
	NC	No connected. This pin should be floating.
MAIN FUNCTION	Main or suggested function.	
COMMENTS	Clarification for the related SMARC interface pin. See device chapter for more information.	

Table 4 SMARC expansion interface information

COLORS	INFORMATION
	Power Sources (Supply Voltages)
	Signal Level Voltage (Digital and Analog Ground)
	Control Signals
	Ethernet
	USB connections
	I2C
	SPI
	Wifi/Bluetooth and SD/SD card interface
	UART
	I2S
	CAN bus
	GPIOs
	Analog Inputs
	DVI
	LCD
	RTC Battery

Table 5 Colors Key

The following table includes all the pins and its description. Please, be careful with the name of pins related to Primary (Top side, pins PXXX) and Secondary (Bottom side, pins SXXX) sides of SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
Primary (Top) Side				
P1	NC	NC	Not connected	Not connected
P2	GND	Power	GND	Digital ground
P3	1V8	IO	CSI1_CK	GPIO4_IO21 (pcam_d0) (1)
P4	NC	NC	Not connected	Not connected (pcam_d1) (1) (2)
P5	NC	NC	Not connected	Not connected
P6	1V8	Input	CSI1_MCLK	GPIO4_IO17 (pcam_mck) (1)
P7	1V8	IO	CSI1_D0+	GPIO4_IO23 (pcam_d2) (1)
P8	1V8	IO	CSI1_D0-	GPIO4_IO24 (pcam_d3) (1)
P9	GND	Power	GND	Digital ground
P10	1V8	IO	CSI1_D1+	CSI1 D1 differential data input. (pcam_d4) (1) (2)
P11	1V8	IO	CSI1_D1-	CSI1 D1 differential data input. (pcam_d5) (1) (2)
P12	GND	Power	GND	Digital ground
P13	1V8	IO	CSI1_D2+	CSI1 D2 differential data input. (pcam_d6) (1) (2)
P14	1V8	IO	CSI1_D2-	CSI1 D2 differential data input. (pcam_d7) (1) (2)
P15	GND	Power	GND	Digital ground
P16	NC	NC	Not connected	Not connected
P17	NC	NC	Not connected	Not connected
P18	GND	Power	GND	Digital ground
P19	NC	NC	Not connected	Not connected
P20	NC	NC	Not connected	Not connected
P21	3V3	Output OD	PHY0_LINK100#	Link Speed Indication LED for 100 Mbps. Active low.
P22	NC	NC	Not connected	Not connected
P23	NC	NC	Not connected	Not connected
P24	NC	NC	Not connected	Not connected
P25	3V3	Output OD	PHY0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10 or 100Mbps) Blinks on Activity

P26	PHY MDI	IO	PHY0_MDI1-	Fast Ethernet pair RX to magnetics (Media Dependent Interface) (1)
P27	PHY MDI	IO	PHY0_MDI1+	Fast Ethernet pair RX to magnetics (Media Dependent Interface) (1)
P28	3V3	Output	PHY0_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic.
P29	PHY MDI	IO	PHY 0_MDI0-	Fast Ethernet pair TX to magnetics (Media Dependent Interface). (1)
P30	PHY MDI	IO	PHY 0_MDI0+	Fast Ethernet pair TX to magnetics (Media Dependent Interface). (1)
P31	NC	NC	Not connected	Not connected
P32	GND	Power	GND	Digital ground
P33	NC	NC	Not connected	Not connected
P34	3V3	IO	SDIO_CMD	SDIO card 4-bit Interface: Command Line. (3) (4)
P35	3V3	Input	SDIO_CD#	SDIO card 4-bit Interface: Card Detect. (3) (4)
P36	3V3	Output	SDIO_CK	SDIO card 4-bit Interface: Clock. (3) (4)
P37	NC	NC	Not connected	Not connected
P38	GND	Power	GND	Digital ground
P39	3V3	IO	SDIO_D0	SDIO card 4-bit Interface: data path (D0). (3) (4)
P40	3V3	IO	SDIO_D1	SDIO card 4-bit Interface: data path (D1). (3) (4)
P41	3V3	IO	SDIO_D2	SDIO card 4-bit Interface: data path (D1). (3) (4)
P42	3V3	IO	SDIO_D3	SDIO card 4-bit Interface: data path (D3). (3) (4)
P43	1V8	Output	SPI0_CS0#	ECSPI4 Interface: Master Chip Select 0. Active low. (5)
P44	1V8	Output	SPI0_CK	ECSPI4 Interface: Clock. (5)
P45	1V8	Input	SPI0_DIN	ECSPI4 Interface: Master Data Input. (5)
P46	1V8	Output	SPI0_DO	ECSPI4 Interface: Master Data Output. (5)
P47	GND	Power	GND	Digital ground
P48	NC	NC	Not connected	Not connected
P49	NC	NC	Not connected	Not connected
P50	GND	Power	GND	Digital ground
P51	NC	NC	Not connected	Not connected
P52	NC	NC	Not connected	Not connected
P53	GND	Power	GND	Digital ground

P54	NC	NC	Not connected	Not connected
P55	NC	NC	Not connected	Not connected
P56	NC	NC	Not connected	Not connected
P57	NC	NC	Not connected	Not connected
P58	NC	NC	Not connected	Not connected
P59	GND	Power	GND	Digital ground
P60	USB	IO	USB0+	UBS1-OTG: USB2.0 differential data input.
P61	USB	IO	USB0-	UBS1-OTG: USB2.0 differential data input.
P62	3V3	IO OD	USB0_EN_OC#	USB1-OTG: Enable (active High)-Overcurrent (active Low) PIN
P63	5V	Input	USB0_VBUS_DET	USB1-OTG: USB2.0 Host power detection when this port is used as a device.
P64	3V3	Input	USB0_OTG_ID	USB1-OTG: Input Pin to Announce OTG ID (Device Insertion) on USB 2.0 Port.
P65	USB	IO	USB1+	UBS2: USB2.0 differential data input.
P66	USB	IO	USB1-	UBS2: USB2.0 differential data input.
P67	3V3	IO OD	USB1_EN_OC#	USB2: Enable OUT (active High)-Overcurrent IN (active Low) PIN
P68	GND	Power	GND	Digital ground
P69	NC	NC	Not connected	Not connected
P70	NC	NC	Not connected	Not connected
P71	NC	NC	Not connected	Not connected
P72	NC	NC	Not connected	Not connected
P73	NC	NC	Not connected	Not connected
P74	NC	NC	Not connected	Not connected
P75	NC	NC	Not connected	Not connected
P76	NC	NC	Not connected	Not connected
P77	NC	NC	Not connected	Not connected
P78	NC	NC	Not connected	Not connected
P79	GND	Power	GND	Digital ground
P80	NC	NC	Not connected	Not connected
P81	NC	NC	Not connected	Not connected

P82	GND	Power	GND	Digital ground
P83	NC	NC	Not connected	Not connected
P84	NC	NC	Not connected	Not connected
P85	GND	Power	GND	Digital ground
P86	NC	NC	Not connected	Not connected
P87	NC	NC	Not connected	Not connected
P88	GND	Power	GND	Digital ground
P89	NC	NC	Not connected	Not connected
P90	NC	NC	Not connected	Not connected
P91	GND	Power	GND	Digital ground
P92	NC	NC	Not connected	Not connected
P93	NC	NC	Not connected	Not connected
P94	GND	Power	GND	Digital ground
P95	NC	NC	Not connected	Not connected
P96	NC	NC	Not connected	Not connected
P97	GND	Power	GND	Digital ground
P98	NC	NC	Not connected	Not connected
P99	NC	NC	Not connected	Not connected
P100	GND	Power	GND	Digital ground
P101	NC	NC	Not connected	Not connected
P102	NC	NC	Not connected	Not connected
P103	GND	Power	GND	Digital ground
P104	NC	NC	Not connected	Not connected
P105	NC	NC	Not connected	Not connected
P106	NC	NC	Not connected	Not connected
P107	NC	NC	Not connected	Not connected
P108	1V8	IO	GPIO0/CAM0_PWR#	GPIO FROM IOMUX P12 (I2C2)
P109	1V8	IO	GPIO1/CAM1_PWR#	GPIO FROM IOMUX P13 (I2C2)
P110	1V8	IO	GPIO2CAM0_RST#	GPIO FROM IOMUX P14 (I2C2)
P111	1V8	IO	GPIO3/CAM1_RST#	GPIO FROM IOMUX P15 (I2C2)

P112	1V8	IO	GPIO4/HDA_RST#	GPIO FROM IOMUX P16 (I2C2)
P113	1V8	IO	GPIO5/PWM_OUT	GPIO FROM IOMUX P17 (I2C2)
P114	1V8	IO	GPIO6/TACHIN	GPIO FROM IOMUX P20 (I2C2)
P115	1V8	IO	GPIO7/PCAM_FLD	GPIO FROM IOMUX P21 (I2C2)
P116	1V8	IO	GPIO8/CAN0_ERR#	GPIO FROM IOMUX P22 (I2C2)
P117	1V8	IO	GPIO9/CAN1_ERR#	GPIO FROM IOMUX P23 (I2C2)
P118	1V8	IO	GPIO10	GPIO FROM IOMUX P24 (I2C2)
P119	1V8	IO	GPIO11	GPIO FROM IOMUX P25 (I2C2)
P120	GND	Power	GND	Digital ground
P121	1V8	IO OD	I2C_PM_CK	Power management I2C bus CLK
P122	1V8	IO OD	I2C_PM_DAT	Power management I2C bus DATA
P123	1V8	Input	BOOT_SEL0#	Input straps determine the Module boot device. Active low.
P124	1V8	Input	BOOT_SEL1#	Input straps determine the Module boot device. Active low.
P125	1V8	Input	BOOT_SEL2#	Input straps determine the Module boot device. Active low.
P126	1V8	Output	RESET_OUT#	General purpose reset output to Carrier board.
P127	1V8	Input	RESET_IN#	Reset input from Carrier board. Active low.
P128	1V8	Input	POWER_BTN#	ON_OFF signal has been connected to ON_OFF input of microprocessor
P129	1V8	Output	SER0_TX	UART1: Asynchronous serial port 1 data out. (6)
P130	1V8	Input	SER0_RX	UART1: Asynchronous serial port 1 data in. (7)
P131	1V8	Output	SER0_RTS#	UART1: Request to Send handshake line. Active low.
P132	1V8	Input	SER0_CTS#	UART1: Clear to Send handshake line. Active low.
P133	GND	Power	GND	Digital ground
P134	1V8	Output	SER1_TX	UART3: Asynchronous serial port 1 data out.
P135	1V8	Input	SER1_RX	UART3: Asynchronous serial port 1 data in.
P136	1V8	Output	SER2_TX	UART2: Asynchronous serial port 1 data out. (8)
P137	1V8	Input	SER2_RX	UART2: Asynchronous serial port 1 data in. (8)
P138	1V8	Output	SER2_RTS#	UART2: Request to Send handshake line. Active low. (8)
P139	1V8	Input	SER2_CTS#	UART2: Clear to Send handshake line. Active low. (8)

P140	NC	NC	Not connected	Not connected
P141	NC	NC	Not connected	Not connected
P142	GND	Power	GND	Digital ground
P143	1V8	Output	CAN0_TX	CAN1_TX (1)
P144	1V8	Input	CAN0_RX	CAN1_RX (1)
P145	NC	NC	Not connected	Not connected
P146	NC	NC	Not connected	Not connected
P147	3V to 5V25	Power	VDD_IN0	Pins used to power up the module. Source voltage should be between 3V to 5V25
P148	3V to 5V25	Power	VDD_IN1	Pins used to power up the module. Source voltage should be between 3V to 5V25
P149	3V to 5V25	Power	VDD_IN2	Pins used to power up the module. Source voltage should be between 3V to 5V25
P150	3V to 5V25	Power	VDD_IN3	Pins used to power up the module. Source voltage should be between 3V to 5V25
P151	3V to 5V25	Power	VDD_IN4	Pins used to power up the module. Source voltage should be between 3V to 5V25
P152	3V to 5V25	Power	VDD_IN5	Pins used to power up the module. Source voltage should be between 3V to 5V25
P153	3V to 5V25	Power	VDD_IN6	Pins used to power up the module. Source voltage should be between 3V to 5V25
P154	3V to 5V25	Power	VDD_IN7	Pins used to power up the module. Source voltage should be between 3V to 5V25
P155	3V to 5V25	Power	VDD_IN8	Pins used to power up the module. Source voltage should be between 3V to 5V25
P156	3V to 5V25	Power	VDD_IN9	Pins used to power up the module. Source voltage should be between 3V to 5V25
Secondary (Bottom) Side				
S1	1V8	IO	CSI_VSYNC	GPIO4_IO19 (pcam_vsync) (1)
S2	1V8	IO	CSI_HSYNC	GPIO4_IO20 (pcam_hsync) (1)
S3	GND	Power	GND	Digital ground
S4	1V8	IO	CSI_PIXCLK	GPIO4_IO18 (pcam_pxlck) (1)
S5	NC	NC	Not connected	Not connected
S6	NC	NC	Not connected	Not connected
S7	NC	NC	Not connected	Not connected

S8	NC	NC	Not connected	Not connected
S9	NC	NC	Not connected	Not connected
S10	GND	Power	GND	Digital ground
S11	NC	NC	Not connected	Not connected
S12	NC	NC	Not connected	Not connected
S13	GND	Power	GND	Digital ground
S14	NC	NC	Not connected	Not connected
S15	NC	NC	Not connected	Not connected
S16	GND	Power	GND	Digital ground
S17	PHY MDI	IO	PHY 1_MDI0+	Fast Ethernet pair 0 (TX) to magnetics (Media Dependent Interface).(1)
S18	PHY MDI	IO	PHY1_MDI0-	Fast Ethernet pair 0 (TX) to magnetics (Media Dependent Interface).(1)
S19	3V3	Output OD	PHY1_LINK100#	Link Speed indication LED for 100 Mbps. Active low.
S20	PHY MDI	IO	PHY 1_MDI1+	Fast Ethernet pair 1 (RX) to magnetics (Media Dependent Interface).(1)
S21	PHY MDI	IO	PHY1_MDI1-	Fast Ethernet pair 1 (RX) to magnetics (Media Dependent Interface).(1)
S22	NC	NC	Not connected	Not connected
S23	NC	NC	Not connected	Not connected
S24	NC	NC	Not connected	Not connected
S25	GND	Power	GND	Digital ground
S26	NC	NC	Not connected	Not connected
S27	NC	NC	Not connected	Not connected
S28	3V3	Output	PHY1_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic. (1)
S29	3V3	IO	TAMPER0	SNVS_TAMPER0
S30	3V3	IO	TAMPER1	SNVS_TAMPER1
S31	3V3	Output OD	PHY1_LINK_ACT#	Fast Ethernet Link / Activity Indication LED Driven Low on Link (10 or 100Mbps) Blinks on Activity. (1)
S32	3V3	IO	TAMPER2	SNVS_TAMPER2
S33	3V3	IO	TAMPER3	SNVS_TAMPER3
S34	GND	Power	GND	Digital ground

S35	NC	NC	Not connected	Not connected
S36	NC	NC	Not connected	Not connected
S37	NC	NC	Not connected	Not connected
S38	1V8	Output	AUDIO_MCK	SAI1_MCLK: Master Clock output to Audio codecs. (9)
S39	1V8	IO	I2S0_LRCK	SAI1_TX_SYNC: Left & Right Audio synchronization clock. (9)
S40	1V8	Output	I2S0_SDOUT	SAI1_TX_DATA: Digital Audio output. (9)
S41	1V8	Input	I2S0_SDIN	SAI1_RX_DATA: Digital Audio input. (9)
S42	1V8	IO	I2S0_CK	SAI1_TX_BLCK: Digital Audio clock. (9)
S43	NC	NC	Not connected	Not connected
S44	NC	NC	Not connected	Not connected
S45	NC	NC	Not connected	Not connected
S46	NC	NC	Not connected	Not connected
S47	GND	Power	GND	Digital ground
S48	1V8	IO OD	I2C_GP_CK	I2C1: Clock signal.
S49	1V8	IO OD	I2C_GP_DAT	I2C1: Data signal.
S50	1V8	IO	I2S2_LRCK	SAI2_SYNC: Left & Right Audio synchronization clock. (8)
S51	1V8	Output	I2S2_SDOUT	SAI2_TXD: Digital Audio output. (8)
S52	1V8	Input	I2S2_SDIN	SAI2_RXD: Digital Audio input. (8)
S53	1V8	IO	I2S2_CK	SAI2_BCLK: Digital Audio clock. (8)
S54	NC	NC	Not connected	Not connected
S55	3V3	IO	TAMPER9	SNVS_TAMPER9
S56	1V8	Input	ENET2_RXD1	ENET2_RXD1 (10)
S57	NC	NC	Not connected	Not connected
S58	NC	NC	Not connected	Not connected
S59	NC	NC	Not connected	Not connected
S60	NC	NC	Not connected	Not connected
S61	GND	Power	GND	Digital ground
S62	1V8	Output	ENET2_TXD0	ENET2_TXD0 (10)
S63	1V8	Output	ENET2_TXD1	ENET2_TXD1 (10)

S64	GND	Power	GND	Digital ground
S65	1V8	Input	ENET2_RXD0	ENET2_RXD0 (10)
S66	1V8	Output	ENET2_TXEN	ENET2_TXEN (10)
S67	GND	Power	GND	Digital ground
S68	1V8	Output	ENET2_TX_CLK	ENET2_TX_CLK (10)
S69	1V8	Output	ENET2_RXER	ENET2_RXER (10)
S70	GND	Power	GND	Digital ground
S71	1V8	IO	ENET2_MDIO	ENET2_MDIO (10)
S72	1V8	Output	ENET2_MDC	ENET2_MDC (10)
S73	GND	Power	GND	Digital ground
S74	1V8	IO	ENET2_RESETn	ENET2_RESET (10)
S75	NC	NC	Not connected	Not connected
S76	NC	NC	Not connected	Not connected
S77	3V3	IO	TAMPER4	SNVS_TAMPER4
S78	3V3	IO	TAMPER5	SNVS_TAMPER5
S79	3V3	IO	TAMPER6	SNVS_TAMPER6
S80	GND	Power	GND	Digital ground
S81	3V3	IO	TAMPER7	SNVS_TAMPER7
S82	3V3	IO	TAMPER8	SNVS_TAMPER8
S83	GND	Power	GND	Digital ground
S84	NC	NC	Not connected	Not connected
S85	NC	NC	Not connected	Not connected
S86	GND	Power	GND	Digital ground
S87	NC	NC	Not connected	Not connected
S88	NC	NC	Not connected	Not connected
S89	GND	Power	GND	Digital ground
S90	NC	NC	Not connected	Not connected
S91	NC	NC	Not connected	Not connected
S92	GND	Power	GND	Digital ground
S93	1V8	Output	LCD_D0	LCD_DATA00

S94	1V8	Output	LCD_D1	LCD_DATA01
S95	1V8	Output	LCD_D2	LCD_DATA02
S96	1V8	Output	LCD_D3	LCD_DATA03
S97	1V8	Output	LCD_D4	LCD_DATA04
S98	1V8	Output	LCD_D5	LCD_DATA05
S99	1V8	Output	LCD_D6	LCD_DATA06
S100	1V8	Output	LCD_D7	LCD_DATA07
S101	GND	Power	GND	Digital ground
S102	1V8	Output	LCD_D8	LCD_DATA08
S103	1V8	Output	LCD_D9	LCD_DATA09
S104	1V8	Output	LCD_D10	LCD_DATA10
S105	1V8	Output	LCD_D11	LCD_DATA11
S106	1V8	Output	LCD_D12	LCD_DATA12
S107	1V8	Output	LCD_D13	LCD_DATA13
S108	1V8	Output	LCD_D14	LCD_DATA14
S109	1V8	Output	LCD_D15	LCD_DATA15
S110	GND	Power	GND	Digital ground
S111	1V8	Output	LCD_D16	LCD_DATA16
S112	1V8	Output	LCD_D17	LCD_DATA17
S113	1V8	Output	LCD_D18	LCD_DATA18
S114	1V8	Output	LCD_D19	LCD_DATA19
S115	1V8	Output	LCD_D20	LCD_DATA20
S116	1V8	Output	LCD_D21	LCD_DATA21
S117	1V8	Output	LCD_D22	LCD_DATA22
S118	1V8	Output	LCD_D23	LCD_DATA23
S119	GND	Power	GND	Digital ground
S120	1V8	Output	LCD_DE	LCD_ENABLE
S121	1V8	Output	LCD_VS	LCD_VSYNC
S122	1V8	Output	LCD_HS	LCD_HSYNC
S123	1V8	Output	LCD_PCK	LCD_CLK

S124	GND	Power	GND	Digital ground
S125	NC	NC	Not connected	Not connected
S126	NC	NC	Not connected	Not connected
S127	1V8	Output	LCD0_BKLT_EN	LCD Primary Panel Backlight Enable.
S128	NC	NC	Not connected	Not connected
S129	NC	NC	Not connected	Not connected
S130	GND	Power	GND	Digital ground
S131	NC	NC	Not connected	Not connected
S132	NC	NC	Not connected	Not connected
S133	1V8	Output	LCD_VDD_EN	LCD Primary Panel Power Enable.
S134	NC	NC	Not connected	Not connected
S135	NC	NC	Not connected	Not connected
S136	GND	Power	GND	Digital ground
S137	NC	NC	Not connected	Not connected
S138	NC	NC	Not connected	Not connected
S139	1V8	IO	I2C_LCD_CK	I2C Clock signal for LCD.
S140	1V8	IO	I2C_LCD_DAT	I2C Data signal for LCD.
S141	NC	NC	Not connected	Not connected
S142	NC	NC	Not connected	Not connected
S143	GND	Power	GND	Digital ground
S144	NC	NC	Not connected	Not connected
S145	NC	NC	Not connected	Not connected
S146	NC	NC	Not connected	Not connected
S147	3V	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.
S148	NC	NC	Not connected	Not connected
S149	NC	NC	Not connected	Not connected
S150	NC	NC	Not connected	Not connected
S151	NC	NC	Not connected	Not connected
S152	NC	NC	Not connected	Not connected
S153	1V8	Output	CARRIER_STBY#	Standby state.

S154	1V8	Output	CARRIER_PWR_ON#	Signal to enable Carrier Board power on.
S155	1V8	Input	FORCE_RECOV#	Force Recovery
S156	NC	NC	Not connected	Not connected
S157	NC	NC	Not connected	Not connected
S158	GND	Power	GND	Digital ground

Notes

(1)	**Some versions do not support this functionality. Check if microprocessor support this functionality.**
(2)	**PCAM function could be available under demand by deleting I2S0 (SAI1).**
(3)	**This function is only present in No WiFi models (some pins are shared with WiFi SDIO).**
(4)	**In WiFi models this function is available during Boot process only.**
(5)	**Only available on LITE versions without ET2.**
(6)	**It is also connected to TX in JTAG connector.**
(7)	**It is also connected to RX in JTAG connector.**
(8)	**This function is only present in No WiFi models.**
(9)	**This function is not available in case of parallel camera is used.**
(10)	**This function can only be used in versions without PHY1**

Table 6 SMARC pinout description

5 PRODUCT SPECIFICATIONSUMMARY

5.1 POWER SOURCES

5.1.1 Supply Voltage

SMARC iMX6-UL/ULL module cannot be used as stand-alone module, so keep in mind that expansion board must power VIN signal input. This signal is defined into MXM3 314-pin interface (SMARC) and can be in a range between 3V to 5V25. For more information see electrical characteristics table in chapter **¡Error! No se encuentra el origen de la referencia. ¡Error! No se encuentra el origen de la referencia.**.

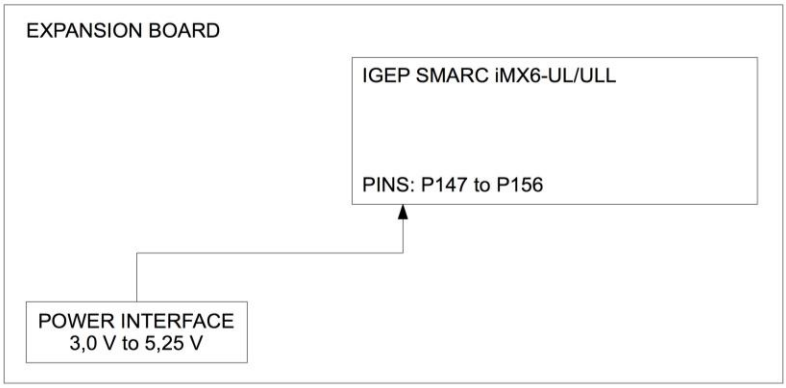

Figure 12 Power Supply Input Diagram

In next table there is a summary all pins of Power Supply available related to the SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
3V to 5V25 Input Power				
P147	3V to 5V25	Power	VDD_IN0	Pins used to power up the module. Source voltage should be between 3V to 5V25
P148	3V to 5V25	Power	VDD_IN1	Pins used to power up the module. Source voltage should be between 3V to 5V25
P149	3V to 5V25	Power	VDD_IN2	Pins used to power up the module. Source voltage should be between 3V to 5V25
P150	3V to 5V25	Power	VDD_IN3	Pins used to power up the module. Source voltage should be between 3V to 5V25
P151	3V to 5V25	Power	VDD_IN4	Pins used to power up the module. Source voltage should be between 3V to 5V25
P152	3V to 5V25	Power	VDD_IN5	Pins used to power up the module. Source voltage should be between 3V to 5V25
P153	3V to 5V25	Power	VDD_IN6	Pins used to power up the module. Source voltage should be between 3V to 5V25
P154	3V to 5V25	Power	VDD_IN7	Pins used to power up the module. Source voltage should be between 3V to 5V25
P155	3V to 5V25	Power	VDD_IN8	Pins used to power up the module. Source voltage should be between 3V to 5V25
P156	3V to 5V25	Power	VDD_IN9	Pins used to power up the module. Source voltage should be between 3V to 5V25

Table 7 Power Supply pins

5.1.2 Digital Ground

All the digital GND pins are internally connected. However, the user has to considerer how many of them should connect according to the total consumption of the complete circuit (SMARC iMX6-UL/ULL and the base board developed). At the same time, to make easier the buses routing, the GND connection chosen should be the nearest to the function used.

It shall be a minimum of 4 GND pins connected, distributed in the most possible equal way along the MXM3 SMARC connector, to get an equalized ground.

In next table there is a summary all pins of GND available related to the MXM3 SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
Digital Ground				
P2	GND	Power	GND	Digital ground
P9	GND	Power	GND	Digital ground
P12	GND	Power	GND	Digital ground
P15	GND	Power	GND	Digital ground
P18	GND	Power	GND	Digital ground
P32	GND	Power	GND	Digital ground
P38	GND	Power	GND	Digital ground
P47	GND	Power	GND	Digital ground
P50	GND	Power	GND	Digital ground
P53	GND	Power	GND	Digital ground
P59	GND	Power	GND	Digital ground
P68	GND	Power	GND	Digital ground
P79	GND	Power	GND	Digital ground
P82	GND	Power	GND	Digital ground
P85	GND	Power	GND	Digital ground
P88	GND	Power	GND	Digital ground
P91	GND	Power	GND	Digital ground
P94	GND	Power	GND	Digital ground
P97	GND	Power	GND	Digital ground
P100	GND	Power	GND	Digital ground
P103	GND	Power	GND	Digital ground
P120	GND	Power	GND	Digital ground

P133	GND	Power	GND	Digital ground
P142	GND	Power	GND	Digital ground
S3	GND	Power	GND	Digital ground
S10	GND	Power	GND	Digital ground
S13	GND	Power	GND	Digital ground
S16	GND	Power	GND	Digital ground
S25	GND	Power	GND	Digital ground
S34	GND	Power	GND	Digital ground
S47	GND	Power	GND	Digital ground
S61	GND	Power	GND	Digital ground
S64	GND	Power	GND	Digital ground
S67	GND	Power	GND	Digital ground
S70	GND	Power	GND	Digital ground
S73	GND	Power	GND	Digital ground
S80	GND	Power	GND	Digital ground
S83	GND	Power	GND	Digital ground
S86	GND	Power	GND	Digital ground
S89	GND	Power	GND	Digital ground
S92	GND	Power	GND	Digital ground
S101	GND	Power	GND	Digital ground
S110	GND	Power	GND	Digital ground
S119	GND	Power	GND	Digital ground
S124	GND	Power	GND	Digital ground
S130	GND	Power	GND	Digital ground
S136	GND	Power	GND	Digital ground
S143	GND	Power	GND	Digital ground
S158	GND	Power	GND	Digital ground

Table 8 Digital Ground pins

5.2 CONTROL SIGNALS

There are different pins used as general control signals. They are related to Boot Mode, Reset functions, the use of an External Pushbutton and some pins related with the Module State Pins.

5.2.1 Boot Modes

There are three pins in the MXM3 SMARC connector which can be used to fix the boot mode of the module (pins 123 to 125 on Top side). They are active low. With them is possible to fix from which device will boot up the module. Next table offers all possible ways.

BOOT2 (P125)	BOOT1 (P124)	BOOT0 (P123)	BOOT MODE
0	0	0	RESERVED
0	0	1	Carrier SD Card
0	1	0	RESERVED
0	1	1	RESERVED
1	0	0	RESERVED
1	0	1	Remote boot (Network (GBE) or Serial)
1	1	0	Module eMMC Flash
1	1	1	RESERVED

Table 9 Boot Mode pins

Reserved positions are combinations which are not implemented in current SMARC module. Users must avoid using them since it would not be possible to complete a module boot up.

Please, be careful that **default position is '111'**. This is a reserved position and it is not possible to perform a complete module boot up since there is not an implemented Flash-SPI at Boot instructions. The User must use any of available combinations. In example, it is possible to boot from a SD-Card using combination '001'.

It is recommended to use a jumper header or a switch in series with a low resistor value (as a short circuit protector element) tied to GND in Carrier Board to control the values of these pins.

5.2.2 Reset pins

There are also two different Reset-IO possibilities. The first one is a General Reset RESET_OUT# (P126) and the other one is a RESET_IN# (P127).

Pin RESET_OUT# (P126) is general purpose reset output to Carrier Board. Related to LCD_RESET.

Pin RESET_IN# (P127) is a reset input from Carrier Board. In this case, when it is low state, Carrier forces a Module Reset.

5.2.3 External Pushbutton

Pin POWER_BTN# (P128) is to be used as Power-button input from Carrier Board. This is active low.

5.2.4 Module State Pins

- **Carrier Standby**

Pin CARRIER_STBY# (S153) - Signal is Low when system is in standby power state.

- **Carrier Power On**

Pin CARRIER_PWR_ON# (S154) - Carrier board circuits (apart from power management and power path circuits) should not be powered until the Module asserts this signal.

- **Force Recovery**

Pin FORCE_RECOV# (S155) - Low on this pin allows non-protected segments of Module boot device to be rewritten/restored from an external USB Host on Module USB0.

The table below shows a summary of all control signals:

Pin	Volt Level	Type	Main Function	Comments
Boot Modes				
P123	1V8	Input	BOOT_SEL0#	Input straps determine the Module boot device. Active low.
P124	1V8	Input	BOOT_SEL1#	Input straps determine the Module boot device. Active low.
P125	1V8	Input	BOOT_SEL2#	Input straps determine the Module boot device. Active low.
Reset functions				
P126	1V8	Output	RESET_OUT#	General purpose reset output to Carrier board.
P127	1V8	Input	RESET_IN#	Reset input from Carrier board. Active low.
External pushbutton				
P128	1V8	Input	POWER_BTN#	ON_OFF signal has been connected to ON_OFF input of microprocessor.
State pins				
S153	1V8	Output	CARRIER_STBY#	Standby state.
S154	1V8	Output	CARRIER_PWR_ON#	Signal to enable Carrier Board power on.
S155	1V8	Input	FORCE_RECOV#	Force Recovery

Table 10 Control Signals pins

5.3 ETHERNET

There are two available Fast Ethernet port in the module (10/100 Mbps). The module implements respective physical layers for each interface and a block of pins of SMARC interface that can be connected directly to the Ethernet connectors. Both transmission and reception lines (TX and RX) are differential (there are a total of four pairs for each Ethernet, and in the pin function is indicated the Negative and Positive) and they should be connected to magnetics for isolation. The data lines must be equal length and symmetric and respect a 100 Ω differential impedance in the layout traces. The differential pairs must be isolated.

Moreover, the magnetics module has a critical effect, so it must be designed carefully. In order to obtain a smaller size, it is usual to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they must respect a separation under of 25 mm between them and the RJ45 connector, and 20 mm or greater between them and the SMARC connector.

There is also possible to connect two LEDs. They are used to indicate the good functioning of the Ethernet connection. The first one (PHY0_LINK_ACT# and PHY1_LINK_ACT#) indicates the line activity (LED on indicates a valid link; LED blinking when there is data traffic). The second one (PHY0_LINK100# and PHY1_LINK100#)) is a link speed indication for 100 Mbps. These are usually in green and yellow color.

The last used pins are PHY0_CTREF and PHY1_CTREF. There are to be used as reference voltage for Carrier Board Ethernet magnetic (If it is required by the module PHY).

In next table is shown all the Ethernet 10/100 Mbps pins:

Pin	Volt Level	Type	Main Function	Comments
P21	3V3	Output OD	PHY0_LINK100#	Link Speed Indication LED for 100 Mbps
P25	3V3	Output OD	PHY 0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10 or 100Mbps) Blinks on Activity
P26	PHY MDI	IO	PHY0_MDI1-	Fast Ethernet pair RX to magnetics (Media Dependent Interface) (1)
P27	PHY MDI	IO	PHY0_MDI1+	Fast Ethernet pair RX to magnetics (Media Dependent Interface) (1)
P28	3V3	Output	PHY0_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic.
P29	PHY MDI	IO	PHY0_MDI0-	Fast Ethernet pair TX to magnetics (Media Dependent Interface). (1)
P30	PHY MDI	IO	PHY0_MDI0+	Fast Ethernet pair TX to magnetics (Media Dependent Interface). (1)
S17	PHY MDI	IO	PHY1_MDI0+	Fast Ethernet pair 0 (TX) to magnetics (Media Dependent Interface). (1)
S18	PHY MDI	IO	PHY1_MDI0-	Fast Ethernet pair 0 (TX) to magnetics (Media Dependent Interface). (1)
S19	3V3	Output OD	PHY1_LINK100#	Link Speed indication LED for 100 Mbps.
S20	PHY MDI	IO	PHY1_MDI1+	Fast Ethernet pair 1 (RX) to magnetics (Media Dependent Interface). (1)

S21	PHY MDI	IO	PHY1_MDI1-	Fast Ethernet pair 1 (RX) to magnetics (Media Dependent Interface). (1)
S28	3V3	Output	PHY1_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic. (1)
S31	3V3	Output OD	PHY1_LINK_ACT#	Fast Ethernet Link / Activity Indication LED Driven Low on Link (10 or 100 Mbps) Blinks on Activity. (1)

Table 11 Ethernet 10/100 Mbps pins

Some versions do not support the second Ethernet. Please, check if processor support this functionality.

In versions that support it but without the second Ethernet physical layer (PHY1) implemented, are available the RGMII outputs and Users can add in their Carrier Boards the PHY to obtain this second Ethernet connection. To match this feature, there has been used a part of the SMARC output which were not used for standard SMARC features. These pins are collected in next table.

Pin	Volt Level	Type	Main Function	Comments
S56	1V8	Input	ENET2_RXD1	ENET2_RXD1 (10)
S62	1V8	Output	ENET2_TXD0	ENET2_TXD0 (10)
S63	1V8	Output	ENET2_TXD1	ENET2_TXD1 (10)
S65	1V8	Input	ENET2_RXD0	ENET2_RXD0 (10)
S66	1V8	Output	ENET2_TXEN	ENET2_TXEN (10)
S68	1V8	Output	ENET2_TX_CLK	ENET2_TX_CLK (10)
S69	1V8	Output	ENET2_RXER	ENET2_RXER (10)
S71	1V8	IO	ENET2_MDIO	ENET2_MDIO (10)
S72	1V8	Output	ENET2_MDC	ENET2_MDC (10)
S74	1V8	IO	ENET2_RESETn	ENET2_RESET (10)

Table 12 ENET pins related to PHY1

5.4 USB CONNECTIONS

There are available two USB 2.0 connections in the module. Because mandatory interfaces in SMARC are USB1 and USB2, these are configured as OTG (On-The-Go) and Host respectively.

- **USB 3.0 OTG**

The USB 2.0 OTG connection allows the configuration of the board as Host or Client in function of the connection wire used for linking both devices (SMARC iMX6-UL/ULL and external device).

There is used the differential pair USB0 as USB 2.0 connection pins.

Control lines are USB0_OTG_ID (to detect what kind of device is connected; active high) and USB0_VBUS_DET (host power detection, when this port is used as a device).

The last used pin is USB0_EN_OC#, who acts as enable bidirectional pin. Be careful when implement over-current function to avoid any short-circuit in this pin.

- **USB 3.0 Host:**

The second USB connection uses differential pair USB1 as USB 2.0 Host.

This port must be Host and there are not used the pins type VBUS_DET and OTG_ID (it is not possibility to have a speed OTG detection by hardware; anyway, it is also possible to have the OTG functions, Host and Client, configured by software).

Be careful, when implement over-current function, to avoid any short circuit in pin USB1_EN_OC#.

Following table offers the list of related pins in the SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
USB 2.0 OTG				
P60	USB	IO	USB0+	UBS1-OTG: USB2.0 differential data input.
P61	USB	IO	USB0-	UBS1-OTG: USB2.0 differential data input.
P62	3V3	IO OD	USB0_EN_OC#	USB1-OTG: Enable (active High)-Overcurrent (active Low) PIN
P63	5V	Input	USB0_VBUS_DET	USB1-OTG: USB2.0 Host power detection when this port is used as a device.
P64	3V3	Input	USB0_OTG_ID	USB1-OTG: Input Pin to Announce OTG ID (Device Insertion) on USB 2.0 Port.
USB 2.0 Host				
P65	USB	IO	USB1+	UBS2: USB2.0 differential data input.
P66	USB	IO	USB1-	UBS2: USB2.0 differential data input.
P67	3V3	IO OD	USB1_EN_OC#	USB2: Enable OUT (active High)-Overcurrent IN(active Low) PIN

Table 13 USB pins

5.5 I2C: INTER-INTEGRATED CIRCUIT INTERFACE

The SMARC iMX6-UL/ULL module can be connected to other peripheral devices using functionality of a standard I2C master and slave. I2C is a two wire, bidirectional serial bus which offers an easy interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.
There are four I2C ports and, according the SMARC standard, all of them has a primary purpose and an alternate use.

- **I2C_PM (I2C 1)**

To be used, as primary purpose, in Power Management functions. A usual function is to control a serial EEPROM in the Carrier Board allowing to read Carrier Board parameters.

- **I2C_GP (I2C 2)**

General purpose I2C bus. This bus is sharing I2C1 with I2C_PM.

- **I2C_LCD (I2C 2)**

LCD display support usually used to read LCD display EDID EEPROMs. It can be considered as a I2C general purpose bus in alternate use.

Next table shows all the I2C pins:

Pin	Volt Level	Type	Main Function	Comments
P121	1V8	IO OD	I2C_PM_CK	Power management I2C bus CLK
P122	1V8	IO OD	I2C_PM_DAT	Power management I2C bus DATA
S48	1V8	IO OD	I2C_GP_CK	I2C1: Clock signal.
S49	1V8	IO OD	I2C_GP_DAT	I2C1: Data signal.
S139	1V8	IO	I2C_LCD_CK	I2C Clock signal for LCD.
S140	1V8	IO	I2C_LCD_DAT	I2C Data signal for LCD.

Table 14 I2C pins

5.6 SPI: SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is one more of the different possibilities to connect the module to external peripherals. The SMARC iMX6-UL/ULL module uses the Enhanced Configurable Serial Peripheral Interface (ECSPI). This is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

SMARC iMX6-UL/ULL uses a 1,8 V voltage levels for ECSPI buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs. **This function is only available in models without ETHERNET2.**

The table below show all the SPI pins in the SMARC connector:

Pin	Volt Level	Type	Main Function	Comments
SPI0				
P43	1V8	Output	SPI0_CS0#	ECSPI4 Interface: Master Chip Select 0. Active low. (5)
P44	1V8	Output	SPI0_CK	ECSPI4 Interface: Clock. (5)
P45	1V8	Input	SPI0_DIN	ECSPI4 Interface: Master Data Input. (5)
P46	1V8	Output	SPI0_DO	ECSPI4 Interface: Master Data Output. (5)

Table 15 SPI pins

5.7 WiFi/Bluetooth and SD/MMC/SDIO CARD (4 bit) INTERFACE

The SMARC iMX6-UL/ULL modules contains a certified high-performance WiFi/Bluetooth module with Texas Instruments chipset. Main features are next:

- IEEE 802.11 b/g/n.
- Bluetooth 4.2.
- Module has an internal antenna.
- Possible to use an external antenna through U.FL jack connector.
- Using external antenna, the cable connected to module must have 50 Ω impedance.

This feature uses control lines from iMX6-UL/ULL processor which are shared with other peripheral.

- **UART2**

This is used to communicate with Bluetooth signals in the WiFi/Bluetooth module (BT_RX, BT_CTS, BT_TX and BT_RTS). If there is not implemented the WiFi/Bluetooth functionality, this can be used as SER2. These pins in the SMARC should float if WiFi/Bluetooth is implemented.

- **SD1 interface**

This can be used, through a switch, to the SDIO input/outputs in the WiFi/Bluetooth module. If there is not implemented, it will be available in the SMARC interface as SDIO interface. These pins should be float if WiFi/Bluetooth is implemented.

In models without WiFi/Bluetooth, it is possible to use the SD/MMC/SDIO interface to install a micro-SD card reader on the Carrier Board. This controller can only support up to 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 8 V and 3.3 V operation, but do not support 1.2 V operation.
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode.
- Up to SDR104 rate.

The use of a micro-SD, because this function shares some pins with WiFi/Bluetooth SDIO, is only present in all models without WiFi/Bluetooth connectivity and in models with WiFi/Bluetooth connectivity during Boot process.

Voltage level for these pins is 3,3 V, so it can be necessary to use level adapters for those SD-cards with a 1,8 V I/O level voltage.

The table below show all the SPI pins in the SMARC connector:

Pin	Volt Level	Type	Main Function	Comments
P34	3V3	I/O CMOS	SDIO_CMD	SDIO card 4-bit Interface: Command Line.
P35	3V3	I OD CMOS	SDIO_CD#	SDIO card 4-bit Interface: Card Detect.
P36	3V3	O CMOS	SDIO_CK	SDIO card 4-bit Interface: Clock.
P39	3V3	I/O CMOS	SDIO_D0	SDIO card 4-bit Interface: data path (D0).
P40	3V3	I/O CMOS	SDIO_D1	SDIO card 4-bit Interface: data path (D1).
P41	3V3	I/O CMOS	SDIO_D2	SDIO card 4-bit Interface: data path (D2).
P42	3V3	I/O CMOS	SDIO_D3	SDIO card 4-bit Interface: data path (D3).

Table 16 SDIO Card Interface pins

5.8 UART: ASYNCHRONOUS SERIAL PORTS

There are up to three asynchronous serial ports defined, some of which are shared with other peripherals. These can be with two or four wires. Available serial ports are next (named according SMARC specification and, in parentheses, the used port from iMX6_UL/ULL processor).

- **SER0 (UART1)**

Four wire port: two data lines and two handshake lines. Please, be careful because pins SER0_TX and SER0_RX are also connected to TX and RX in JTAG.

- **SER1 (UART2)**

Two wire port (data only).

- **SER2 (UART3)**

Four wire port. It is only present in all models without WiFi/Bluetooth connectivity (see also chapter 5.7 WiFi/BLUETOOTH AND SD/MMC/SDIO CARD INTERFACE).

The table below shows all the UART pins:

Pin	Volt Level	Type	Main Function	Comments
P129	1V8	Output	SER0_TX	UART1: Asynchronous serial port 1 data out.
P130	1V8	Input	SER0_RX	UART1: Asynchronous serial port 1 data in.
P131	1V8	Output	SER0_RTS#	UART1: Request to Send handshake line. Active low.
P132	1V8	Input	SER0_CTS#	UART1: Clear to Send handshake line. Active low.
P134	1V8	Output	SER1_TX	UART2: Asynchronous serial port 1 data out.
P135	1V8	Input	SER1_RX	UART2: Asynchronous serial port 1 data in.
P136	1V8	Output	SER2_TX	UART3: Asynchronous serial port 1 data out.
P137	1V8	Input	SER2_RX	UART3: Asynchronous serial port 1 data in.
P138	1V8	Output	SER2_RTS#	UART3: Request to Send handshake line. Active low.
P139	1V8	Input	SER2_CTS#	UART3: Clear to Send handshake line. Active low.

Table 17 Asynchronous Serial Ports pins

5.9 I2S: SERIAL AUDIO PORT

There are up to two I2S (Inter IC Sound) interfaces defined, which provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization and codec/DSP interfaces. SAI key features are the following:

- Transmitter with independent Bit Clock and Frame Sync supporting 1 data line.
- Receiver with independent Bit Clock and Frame Sync supporting 1 data line.
- Maximum Frame Size of 32 Words.
- Word size programmable from 8-bits to 32-bits.
- Word size configured separately for first word and remaining words in frame.
- Asynchronous FIFO for each Transmit and Receive data line.
- Graceful restart after FIFO Error.

There are two I2S interfaces defined. These are used for digital audio I/O and all of them have a common audio master clock signal defined.

Please, be careful because SMARC iMX6-UL/ULL versions using Parallel Camera lost one I2S port (I2S0).

The following table includes all the I2S pins:

Pin	Volt Level	Type	Main Function	Comments
S38	1V8	O CMOS	AUDIO_MCK	SAI1_MCLK: Master Clock output to Audio codecs.
S39	1V8	I/O CMOS	I2S0_LRCK	SAI1_TX_SYNC: Left & Right Audio synchronization clock.
S40	1V8	O CMOS	I2S0_SDOUT	SAI1_TX_DATA: Digital Audio output.
S41	1V8	I CMOS	I2S0_SDIN	SAI1_RX_DATA: Digital Audio input.
S42	1V8	I/O CMOS	I2S0_CK	SAI1_TX_BCLK: Digital Audio clock.
S50	1V8	I/O CMOS	I2S2_LRCK	SAI2_SYNC: Left & Right Audio synchronization clock.
S51	1V8	O CMOS	I2S2_SDOUT	SAI2_TXD: Digital Audio output.
S52	1V8	I CMOS	I2S2_SDIN	SAI2_RXD: Digital Audio input.
S53	1V8	I/O CMOS	I2S2_CK	SAI2_BCLK: Digital Audio clock.

Table 18 I2S Interface pins

5.10 CAN BUS: CONTROLLER AREA NETWORK

The SMARC iMX6-UL/ULL can be integrated in a global system using the serial standard CAN bus. The CAN bus is a standard designed to allow microcontrollers and devices to communicate with each other without a host computer. It is a differential half duplex data bus, using shielded or unshielded twisted pair wiring, with an impedance termination of 120 W at the endpoint of the bus. Nodes on the bus are arranged in daisy-chain fashion.

Some versions do not support this feature. Please, check if microprocessor supports this functionality.

A CAN transceiver is needed on the baseboard to connect the system to the CAN bus.

Some models of processors have not available CAN Bus feature. **Please, contact with Sales Department to check if this is available according to your preferences.**

Pin	Volt Level	Type	Main Function	Comments
P143	1V8	Output	CAN0_TX	CAN1_TX (1)
P144	1V8	Input	CAN0_RX	CAN1_RX (1)

Table 19 CAN BUS pins

5.11 LCD CONTROLER

The SMARC iMX6-UL/ULL has available a parallel data bus of 24-lanes to control a LCD screen. There are also one I2C line in order to configure the LCD, plus one Power Enable and one Backlight Enable.

Some key features of this LCD interface are next:

- Bus master interface to source frame buffer data for display refresh and a DMA interface to manage input data transfers from the LCD requiring minimal CPU overhead.
- 8/16/18/24 bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

Common mode capacitors could be added (optionally) between video data lines and GND for high frequency noise attenuation. Typical capacitance values should be between 22 pF and 47 pF.

Low resistance capacitors should be necessary to protect overshoot voltage. It can be solved using a 10 W series resistor to data and clock lines.

The table below shows all the generic signals to control a LCD in the SMARC connector on SMARC iMX6-UL/ULL:

Pin	Volt Level	Type	Main Function	Comments
S93	1V8	Output	LCD_D0	LCD_DATA00
S94	1V8	Output	LCD_D1	LCD_DATA01
S95	1V8	Output	LCD_D2	LCD_DATA02
S96	1V8	Output	LCD_D3	LCD_DATA03
S97	1V8	Output	LCD_D4	LCD_DATA04
S98	1V8	Output	LCD_D5	LCD_DATA05
S99	1V8	Output	LCD_D6	LCD_DATA06
S100	1V8	Output	LCD_D7	LCD_DATA07
S102	1V8	Output	LCD_D8	LCD_DATA08

S103	1V8	Output	LCD_D9	LCD_DATA09
S104	1V8	Output	LCD_D10	LCD_DATA10
S105	1V8	Output	LCD_D11	LCD_DATA11
S106	1V8	Output	LCD_D12	LCD_DATA12
S107	1V8	Output	LCD_D13	LCD_DATA13
S108	1V8	Output	LCD_D14	LCD_DATA14
S109	1V8	Output	LCD_D15	LCD_DATA15
S111	1V8	Output	LCD_D16	LCD_DATA16
S112	1V8	Output	LCD_D17	LCD_DATA17
S113	1V8	Output	LCD_D18	LCD_DATA18
S114	1V8	Output	LCD_D19	LCD_DATA19
S115	1V8	Output	LCD_D20	LCD_DATA20
S116	1V8	Output	LCD_D21	LCD_DATA21
S117	1V8	Output	LCD_D22	LCD_DATA22
S118	1V8	Output	LCD_D23	LCD_DATA23
S120	1V8	Output	LCD_DE	LCD_ENABLE
S121	1V8	Output	LCD_VS	LCD_VSYNC
S122	1V8	Output	LCD_HS	LCD_HSYNC
S123	1V8	Output	LCD_PCK	LCD_CLK
S127	1V8	Output	LCD0_BKLT_EN	LCD Primary Panel Backlight Enable.
S133	1V8	Output	LCD_VDD_EN	LCD Primary Panel Power Enable.
S139	1V8	IO	I2C_LCD_CK	I2C Clock signal for LCD.
S140	1V8	IO	I2C_LCD_DAT	I2C Data signal for LCD.

Table 20 LCD CONTROLER pins

5.12 MIPI-CSI: CAMERA SERIAL INTERFACE

There are defined two MIPI-CSI camera serial interfaces. Both support MIPI-CSI 2.0 but they are also prepared to support MIPI-CSI 3.0. Main difference is that MIPI-CSI 2.0 uses an I2C bus to communicate with camera (pins I2C_CAM[0:1]) and MIPI-CSI 3.0 uses a differential data lane (alternative function of the same pins, CSI[0:1]_TX+/-).

These two buses are implemented with 2 lanes (CSI0) and up to 4 lanes (CSI1). For each bus, there are also available two lines of Power Enable and Reset, in shared pins with GPIOs. We can see all these pins in the table below:

Pin	Volt Level	Type	Main Function	Comments
P3	1V8	IO	CSI1_CK+	GPIO4_IO21 (pcam_d0) (1)
P4	NC	NC	Not connected	Not connected (pcam_d1) (1) (2)
P6	1V8	Input	CSI1_MCLK	GPIO4_IO17 (pcam_mck) (1)
P7	1V8	IO	CSI1_D0+	GPIO4_IO23 (pcam_d2) (1)
P8	1V8	IO	CSI1_D0-	GPIO4_IO24 (pcam_d3) (1)
P10	1V8	IO	CSI1_D1+	CSI1 D1 differential data input. (pcam_d4) (1) (2)
P11	1V8	IO	CSI1_D1-	CSI1 D1 differential data input. (pcam_d5) (1) (2)
P13	1V8	IO	CSI1_D2+	CSI1 D2 differential data input. (pcam_d6) (1) (2)
P14	1V8	IO	CSI1_D2-	CSI1 D2 differential data input. (pcam_d7) (1) (2)
S1	1V8	IO	CSI_VSYNC	GPIO4_IO19 (pcam_vsync) (1)
S2	1V8	IO	CSI_HSYNC	GPIO4_IO20 (pcam_hsync) (1)
S4	1V8	IO	CSI_PIXCLK	GPIO4_IO18 (pcam_pxlck) (1)
Notes				
(1)	**Some versions do not support this functionality. Check if microprocessor support this functionality.**			
(2)	**PCAM function could be available under demand by deleting I2S0 (SAI1).**			

Table 21 MIPI-CSI pins

5.13 GPIO: GENERAL PURPOSE INPUT OUTPUT

GPIOs are input/output (IO) general purpose pins used to control LEDs, relays, switch, etc. These can be configured as either inputs or outputs.

- When configured as an output: It is possible to write an internal register to control the state driven on the output pin.
- When configured as an input: It is possible to detect the state of the input by reading the state of an internal register.

Pin	Volt Level	Type	Main Function	Comments
P108	1V8	IO	GPIO0/CAM0_PWR#	GPIO FROM IOMUX P12 (I2C2)
P109	1V8	IO	GPIO1/CAM1_PWR#	GPIO FROM IOMUX P13 (I2C2)
P110	1V8	IO	GPIO2CAM0_RST#	GPIO FROM IOMUX P14 (I2C2)
P111	1V8	IO	GPIO3/CAM1_RST#	GPIO FROM IOMUX P15 (I2C2)
P112	1V8	IO	GPIO4/HDA_RST#	GPIO FROM IOMUX P16 (I2C2)
P113	1V8	IO	GPIO5/PWM_OUT	GPIO FROM IOMUX P17 (I2C2)
P114	1V8	IO	GPIO6/TACHIN	GPIO FROM IOMUX P20 (I2C2)
P115	1V8	IO	GPIO7/PCAM_FLD	GPIO FROM IOMUX P21 (I2C2)
P116	1V8	IO	GPIO8/CAN0_ERR#	GPIO FROM IOMUX P22 (I2C2)
P117	1V8	IO	GPIO9/CAN1_ERR#	GPIO FROM IOMUX P23 (I2C2)
P118	1V8	IO	GPIO10	GPIO FROM IOMUX P24 (I2C2)
P119	1V8	IO	GPIO11	GPIO FROM IOMUX P25 (I2C2)

Table 22 GPIO pins

5.14 TAMPER

There are ten (10) general purpose input/output pins to be used for security purposes. These are powered since the RTC battery and can function in an independent way. Their functionality is to be used as a hardware security (independent of the application security routines).

This is not a defined function in SMARC standard, this is just an added function provided by ISEE ASSEMBLY TECHNOLOGY using a few pins in the SMARC connector with unused functions. **Please, be careful if you change of processor module to avoid a bad connection.**

Pin	Volt Level	Type	Main Function	Comments
S29	3v3	IO	TAMPER0	SNVS_TAMPER0
S30	3v3	IO	TAMPER1	SNVS_TAMPER1
S32	3v3	IO	TAMPER2	SNVS_TAMPER2
S33	3v3	IO	TAMPER3	SNVS_TAMPER3

S55	3v3	IO	TAMPER9	SNVS_TAMPER9
S77	3v3	IO	TAMPER4	SNVS_TAMPER4
S78	3v3	IO	TAMPER5	SNVS_TAMPER5
S79	3v3	IO	TAMPER6	SNVS_TAMPER6
S81	3v3	IO	TAMPER7	SNVS_TAMPER7
S82	3v3	IO	TAMPER8	SNVS_TAMPER8

Table 23 TAMPER pins

5.15 RTC BATTERY

In the SMARC connector is an input available to use and RTC backup power. The User will implement a Lithium Cell or Super-Cap in a voltage range between 2,0 V and 3,25 V (it is recommended to use a standard Lithium Cell of 3,0 V). This pin can be left open if RTC functions are not required.

The Carrier Board must be implemented the needed circuits to protect against charging by reverse currents.

Pin	Volt Level	Type	Main Function	Comments
S147	3V	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.

Table 24 RTC pin

5.16 ENVIRONMENTAL SPECIFICATION

General Specification	Operating	Non-operating
Industrial grade (E2)	-40ºC to +80ºC	-40ºC to +80ºC

Table 25 Temperature range

Standard modules are available for Industrial grade temperature range. The operating temperature is the maximum measurable temperature on any spot on the module's surface.

- **Humidity**

93% relative Humidity at 40ºC, non-condensing (according to IEC 60068-2-78).

5.17 STANDARDS AND CERTIFICATIONS

- **RoHS**

The SMARC iMX6-UL/ULL is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

- **CE Marking**

The SMARC iMX6-UL/ULL is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950.

- **WEEE Directive**

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

- **Conformal Coating**

Conformal Coating is available for Computer-on-Modules and for validated SMARC modules. Please, contact your local sales or support for further details.

- **EMC**

The SMARC iMX6-UL/ULL is designed and tested following EN55022 standard ("INFORMATION TECHNOLOGY EQUIPMENT. RADIO DISTURBANCE CHARACTERISTICS. LIMITS AND METHODS OF MEASUREMENT").

- **SMARC Form Factor standard**

The SMARC ("Smart Mobility Architecture") is a versatile small form factor computer Module definition targeting application that require low power, low costs and high performance.

5.18 MTBF

The SMARC iMX6-UL/ULL has been designed with a predicted MTBF (Mean Time Before Failure) of >131400 hours (>15 years).

All hardware components are selected with long time industrial reliability parameters. The MTBF prediction of hardware components and temperature stress could be estimated, but the newest devices are very software dependent. So, final application has an important effect on MTBF.

5.19 MECHANICAL SPECIFICATION

- **Module Dimension**

82,00 mm x 50,00 mm x 4,30 mm (high without JTAG connector)

- **Mechanical Drawing**

The next figures show the SMARC iMX6-UL/ULL modules mechanical dimensions:

  - All dimensions are in millimeters.
  - 10-layer Printed Circuit Board size is 82,00 mm x 50,00 mm x 1,15 mm.
  - Mounting holes are provided, one on each corner.

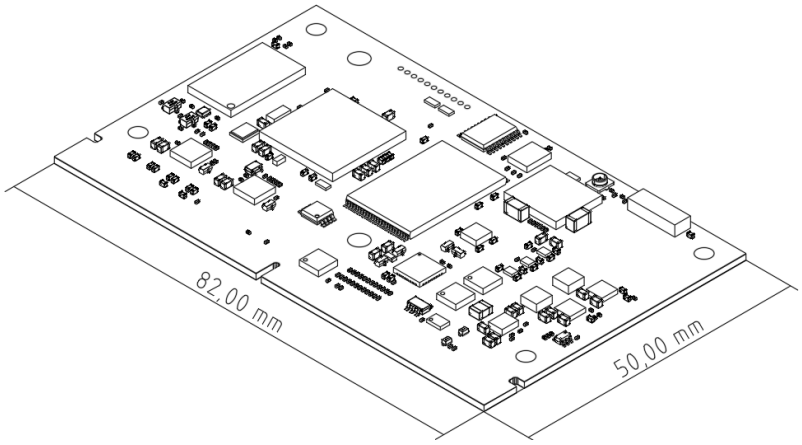

Figure 13 SMARC iMX6-UL/ULL Outline dimensions

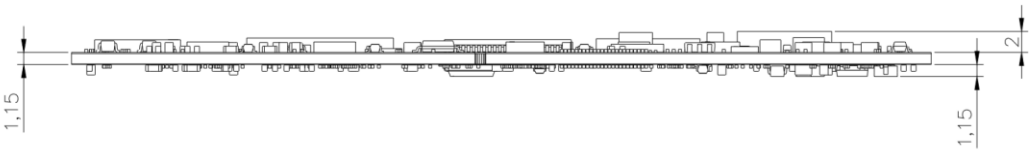

Figure 14 SMARC iMX6-UL/ULL Lateral view widths dimensions

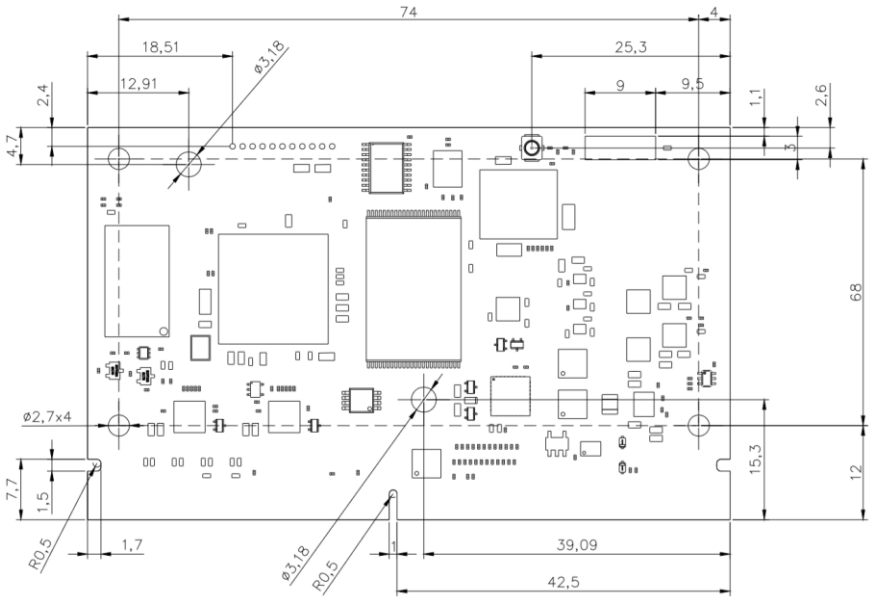

Figure 15 SMARC iMX6-UL/ULL Side view detailed mechanical dimension

6 ON-BOARD INTERFACES

6.1 SUMMARY

Device	Connector	Reference	Description
LEDs	-	LED10MI	GPIO controlled
JTAG	11-pin 1,25 mm pitch interface	JTAG	-

Table 26 Interface summary

6.2 LEDs

The SMARC iMX6-UL/ULL module provides a bicolor LED indicator on the board. It can be controlled by the user through GPIOs.

Signal Name	LED Color	Description
LED_R	LED10MI Red	Controlled by GPIO1_IO08 of iMX6-UL/ULL
LED_G	LED10MI Green	Controlled by GPIO1_IO08 of iMX6-UL/ULL

Table 27 LEDs

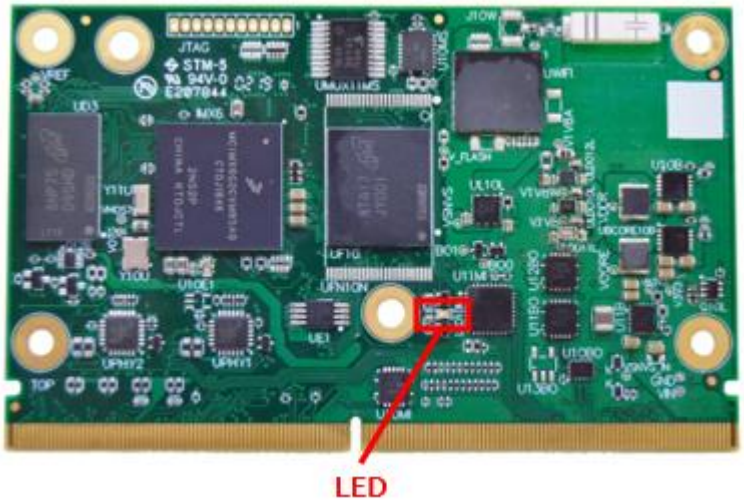

Figure 16 LEDs position in the PCB

6.3 JTAG

The SMARC iMX6-UL/ULL provides a footprint JTAG interface to help in the developing of user's code.

The JTAG port is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG.

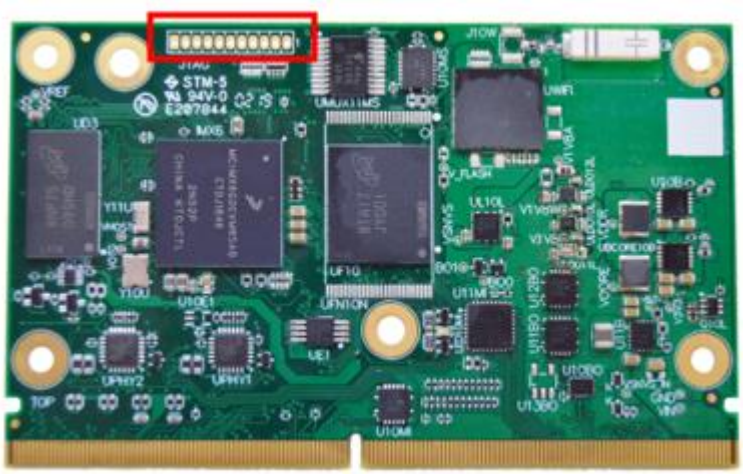

Figure 17 JTAG position in the PCB

Next figure shows the pinout schematic and the corresponding metal contacts.

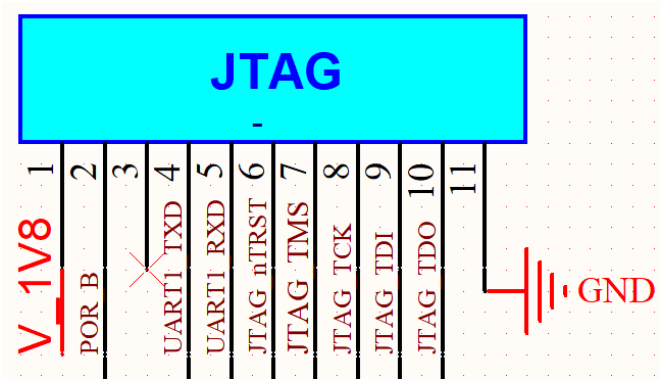

Figure 18 JTAG connector schematic

Note that even pins are left unconnected, but the footprint makes possible to use a 11 pin 1.27 mm pitch connector. Next table details the signals on each pin.

Signal Name	JTAG pin	Description
NVCC_1V8	1	1,8 V power supply.
POR_B	2	Processor iMX6-UL/ULL Cold Reset. Active Low.
NC	3	Not Connected.
UART1_X0	4	UART1: Asynchronous serial port 1 data out.
UART1_X1	5	UART1: Asynchronous serial port 1 data in.
JTAG_NTRST	6	JTAG Test Reset Input Signal.
JTAG_TMS	7	JTAG Test Mode Select Input Signal.
JTAG_TCK	8	JTAG Test Clock Input Signal.
JTAG_TDI	9	JTAG Test Data Input Signal.
JTAG_TDO	10	JTAG Test Data Output Signal.
GND	11	Ground.

Table 28 JTAG pinout

7 ELECTRICAL CHARACTERISTICS

Electrical parameter	Min	Typ	Max	Unit
5 V INPUT POWER SUPPLY				
SMARC iMX6-UL/ULL Input Power Supply Voltage	3.0	-	5.25	V
SMARC iMX6-UL/ULL Input Power Supply Current (1)	-	0.27	2	A
Input/Output pins (2)				
Output High-Level DC Voltage	1.65	-	1.8	V
Input High-Level DC Voltage	1.26	-	1.8	V
Output Low-Level DC Voltage	0	-	0.15	V
Input Low-Level DC Voltage	0	-	0.54	V
RTC_BATTERY type pins				
Input DC Voltage	2.5	3	3.25	V

Table 29 SMARC iMX6-UL/ULL Electrical Characteristics

(1) Current measured with default delivered software. Be aware that different software configurations could drastically modify current consumption.

(2) The electrical specification depends on the configured mode. For accurate information of each pin, revise iMX6-UL/ULL Applications Processor official document from NXP official site https://www.nxp.com/

SMARC iMX6-UL/ULL MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED.

WARRANTY LOST IF IMPROPER USE OF THE MODULE IS FOUND.

8 EXPANSION BOARD

All the products in the SMARC iMX6-UL/ULL series can be supplemented with next expansion board.

Part Number	IGEP™ Device	Description
BASE0040-DFEV-UGAC	BASE SMARC EXPANSION	Designed for fast prototyping of user's projects

Table 30 BASE SMARC EXPANSION Ordering Information

The BASE SMARC EXPANSION is a fully equipped baseboard that access to almost all SMARC functionalities. It has been designed to be used as the fastest way to develop and check the user's final application before building a prototype, saving costs and reducing time to market.

This model can be used with all the ISEE ASSEMBLY TECHNOLOGY's SMARC series modules. Thanks to this design, the user only needs to purchase one Expansion board to check all SMARC modules manufactured by ISEE ASSEMBLY TECHNOLOGY.

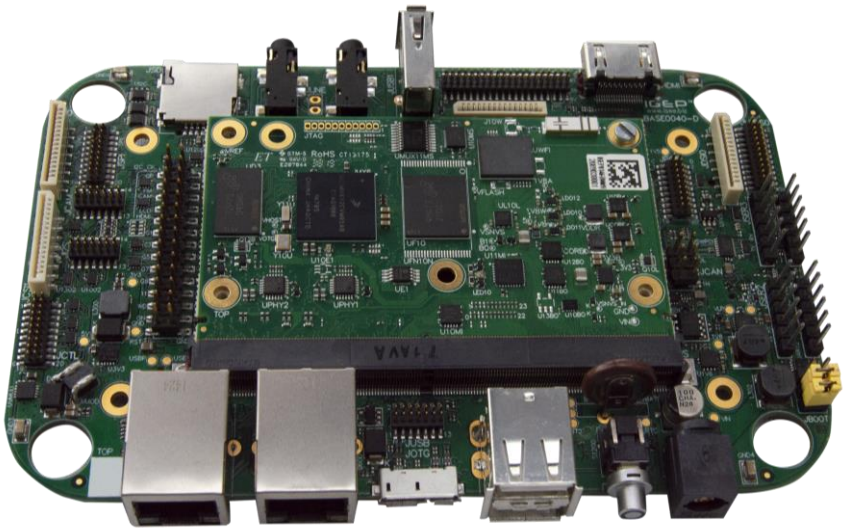

Figure 19 BASE0040 SMARC EXPANSION

The following table contains all the features and capabilities of the BASE SMARC EXPANSION.

Connectors	Features	Dimensions	Case Dimensions
1 x SMARC connector 1 x Power Supply (+5 V) connector 2 x 10/100/1000 Mbps Base RJ45 1 x HDMI Type A receptacle 1 x LCD 24-bit connector 1 x Touchscreen connector 1 x XLCD expansion 40-pin header 1 x LVDS expansion 24-pin header 2 x CSI connector, 2-lanes 1 x Parallel Camera expansion 14-pin header 1 x Stereo Line Input Mic/Line 1 x Stereo Line Output Headphone 1 x I2S 14-pin header 3 x USB 2.0 Type A receptacle 1 x USB 3.0 Type AB receptacle 1 x USB2 expansion 14-pìn header 1 x Modem USB & PCIe interface 1 x mSATA & PCIe interface 1 x PCI expansion 20-pin header 1 x Micro-SD connector 1 x SIM-card connector 2 x DSI connector 2 x CAN on a 6-pin header 1 x SPI 20-pin header 1 x I/O expansion 28-pin header 4 x Serial UART 3V3 expansion 6-pin header	1 x Button-LED (2 LEDs: red, blue) 3 x Boot jumpers 1 x Control 20-pin header	142,00 mm x 90,00 mm (without case)	150,00 mm x 100,00 mm x 30,00 mm

Table 31 BASE0040 SMARC EXPANSION Features Rev. D

9 Document and Standards References

- **CAN** (“Controller Area Network”) Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (https://www.iso.org)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (https://www.iso.org)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (https://www.sae.org)
- **MIPI CSI-2** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **MIPI CSI-3** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **COM Express** – the formal title for the COM Express specification is “PICMG® COM.0 COM Express Module Base Specification”, Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG (“PCI Industrial Computer Manufacturer’s Group”) (www.picmg.org)
- **DisplayPort and Embedded DisplayPort -** These standards are owned and maintained by VESA (“Video Electronics Standards Association”) (www.vesa.org)
- **MIPI DSI** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **eMMC** (“Embedded Multi-Media Card”) The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (www.jedec.org)
- **eSPI** (“Enhanced Serial Peripheral Interface”) The eSPI Interface Base Specification is defined by Intel (https://www.intel.com)
- **Fieldbus** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: https://www.profibus.com/download/ and www.can-cia.org
- **GBE MDI** (“Gigabit Ethernet Medium Dependent Interface”) This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- **HDA (HD Audio),** High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (http://www.intel.com)
- **HDMI Specification,** Version 2.1, November 28, 2017 (www.hdmi.org)
- **I2C Specification,** Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (www.nxp.com)
- **I2S Bus Specification**, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- **IEEE1588 - 2008**. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (http://standards.ieee.org)
- **JTAG** (“Joint Test Action Group”) This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (https://ieeexplore.ieee.org)
- **MXM3** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- **PICMG® EEEP** Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org)
- **PCI Express** Specifications (www.pci-sig.org)
- **Serial ATA** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org) SMARC 2.1.1 Specification © 2020 SGET e.V. Page 9 of 109
- **SD Specifications** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association (“Secure Digital”) (www.sdcard.org)
- **SM Bus** – “System Management Bus” Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (http://www.smbus.org)

- **SPI Bus** – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- **USB** Specifications (http://www.usb.org)