# IGEP ™ COM AQUILA AM335x

# HARDWARE REFERENCE MANUAL

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# 2 INTRODUCTION

## 2.1 PRODUCT DESCRIPTION

The IGEP™ COM AQUILA AM335x is an industrial ultra-low computer module based on ARM Cortex-A8 at speeds up to 1 GHz by Texas Instruments Sitara AM335x family of processors.

It's an industrial computer module (it can work in a temperature range from -40ºC to +85ºC), in a very low profile (its dimensions are only 67,2mm x 26mm). With different combinations of RAM and Flash memory (see the customized possibilities at chapter 2.4), a complete list of interfaces and peripherals including 3D graphic accelerator, it can be the base for a complex industrial equipment or any other kind of application.

There is also an expansion board (IGEP™ COM AQUILA EXPANSION BOARD) to complement the module. It's a development baseboard and it can be used as the fastest way to develop and test the final application before the prototyping phase.

### Highlights:

- Fully tested, highly reliable, scalable, efficient and high performing board that allows customers to focus on their end application.
- Designed for industrial range purposes (temperature range: -40ºC to +85ºC).
- With ultra-compact design and extended temperature range it's adaptable to any custom baseboard.
- Easy connectivity through the SODIMM 200 pin connector. Very small form factor size (67,6x26mm).
- 3V3 I/O level signals.
- MicroSD card reader on-board.
- JTAG interface available.
- It is based on Texas Instruments® AM335x processor which has an advanced Cortex-A8 ARM Architecture version 7 ISA CPU.
- The AM335x Family processors are based on the enhanced device architecture and include the NEON™ Media coprocessor.
- This architecture of high performance applications processor is designed to provide best in class ARM and graphics performance while delivering low power consumption.
- Ka-Ro™ Electronics TX48 Form Factor Compatible.
- 10/100 Mbps Ethernet MAC+PHY interface.
- RTC on board.
- Flexible Memory of Flash Memory combinations (customized option).
- Over Voltage protection.

## 2.2 IGEP™ COM AQUILA AM335x BENEFITS AND APPLICATIONS

There are a lot of advantages that developers will find in the IGEP™ COM AQUILA AM335x series. On broad terms, it's a friendlier way to achieve your projects. Amongst others, the main benefits are the following:

- Compact and powerful core for new products
- Robust and easy to mount due to the SODIMM-200 connector
- Reduced time to market
- Low power consumption ≤ 1,5W
- Industrial Temperature Range -40 to +85ºC.
- Extended life range product (min 10 years)

At the same time, it can be implemented in all kind of end applications. The followings are just a few ones, but the list can be as long as the imagination of the developers.

- Connected vending machines
- Home / Building automation
- Human Interface
- Industrial Control
- Test and Measurement

## 2.3 The IGEP™ COM AQUILA AM335x SERIES

The IGEP™ COM AQUILA AM335x series is composed by a main model and four custom models. They are all made with the same care and quality that ISEE customers already know and trust.

The standard model, IGEP™ COM AQUILA AM3354, is based on the chip AM3354, with a 256 MB DDR3 SDRAM memory and using a 128 MB NandFlash as internal storage memory.

The custom models use another CPU variants (available models: AM3352, AM3358 and AM3359), RAM (up to 512 MB) and NandFlash (up to 512 MB). In the chapter 3.3 are commented the main differences according to processor model. The custom models have a MOQ of 100 units.

## 2.4 ORDERING INFORMATION

| IGEP™ Device | Model Reference | Description |
|---|---|---|
| IGEP™ COM AQUILA AM3354 | IGEP0033-RB1x | Processor: T. I. AM3354BZCZD80 (ARM Cortex-A8)<br>RAM Memory: 256 MB DDR3 SDRAM<br>Storage: 128 MB NANDFLASH |
| **Customized models** | | |
| IGEP™ COM AQUILA AM3352 | IGEP0033-RB2x | Processor: T. I. AM3352BZCZD80 (ARM Cortex-A8)<br>RAM Memory: 128 MB up to 512 MB DDR3 SDRAM<br>Storage: 128 MB up to 512 MB NANDFLASH |
| IGEP™ COM AQUILA AM3354 | IGEP0033-RB3x | Processor: T. I. AM3354BZCZD80 (ARM Cortex-A8)<br>RAM Memory: 512 MB DDR3 SDRAM<br>Storage: 128 MB NANDFLASH |
| IGEP™ COM AQUILA AM3358 | IGEP0033-RB4x | Processor: T. I. AM3358BZCZA80 (ARM Cortex-A8)<br>RAM Memory: 128 MB up to 512 MB DDR3 SDRAM<br>Storage: 128 MB up to 512 MB NANDFLASH |
| IGEP™ COM AQUILA AM3359 | IGEP0033-RB5x | Processor: T. I. AM3359BZCZA80 (ARM Cortex-A8)<br>RAM Memory: 128 MB up to 512 MB DDR3 SDRAM<br>Storage: 128 MB up to 512 MB NANDFLASH |

Table 1 IGEP0033 Ordering Information

## 2.5 EXPANSIONS BOARDS

All the products in the IGEP™ COM AQUILA AM335x series can be supplemented with next expansion board.

| IGEP™ Device | Model Reference | Description |
|---|---|---|
| IGEP™ AQUILA EXPANSION | BASE0033-RA01 | Designed for fast prototyping of user's projects |

Table 2 BASE0033 Ordering Information

# 3 OVERVIEW

## 3.1 IGEP™ COM AQUILA AM335x

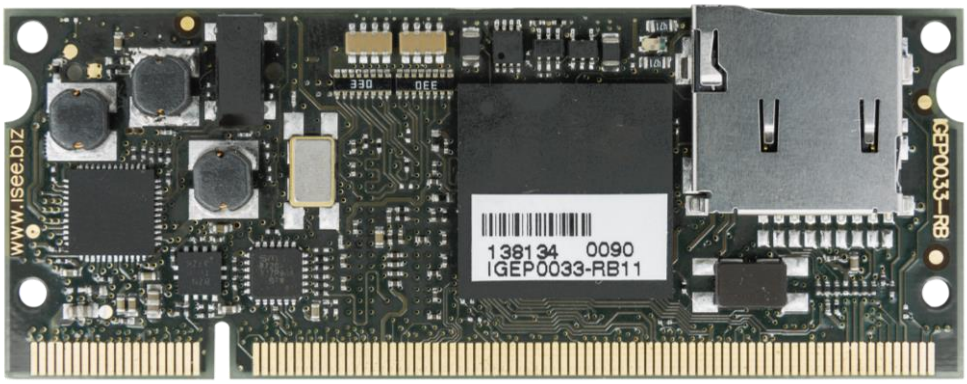


Figure 1 IGEP™ COM AQUILA AM335x – Top View

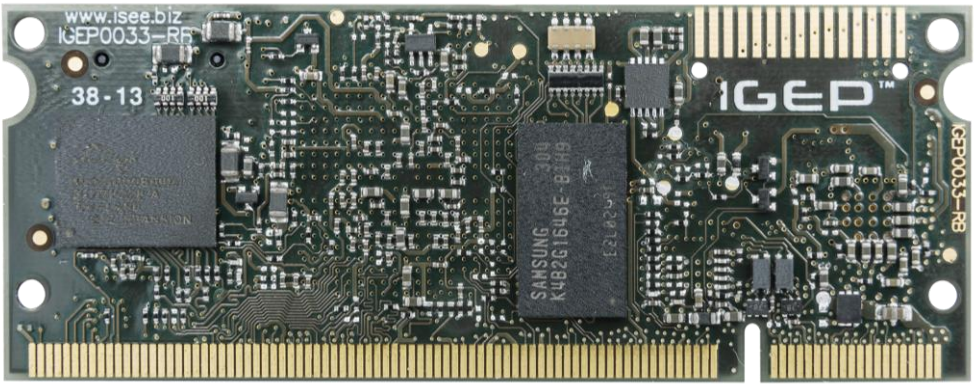


Figure 2 IGEP™ COM AQUILA AM335x – Bottom View

## 3.2 IGEP™ COM AQUILA AM335x FEATURES

| Feature | Specifications |
|---|---|
| IGEP™ COM AQUILA AM335x ARM CPU | Texas Instruments AM335x ARM Cortex–A8™<br>L1 cache: 32 KB (ARM)<br>L2 cache: 256 KB (ARM)<br>NEON™ SIMD Coprocessor<br>DMA, Interrupt controllers, Timers<br>POWERVR© SGX530 3D Graphics (only available for some processors) |
| RAM Memory | 256 MB DDR3 SDRAM, up to 512 MB and 400 MHz clock |
| Storage | 128 MB SLC NANDFLASH up to 512 MB<br>On board micro-SD socket. Can be plugged SDHC cards up to 32 GB. |
| Power to SODIMM-200 connector | Supply Voltage (VIN) from 3.8 V to 5.5 V DC |
| Interfaces | 1 x SODIMM 200-pin expansion interface (DDR1 2V5 compatible)<br>1 x JTAG interface<br>1 x MICRO-SD socket |
| Devices | 1 x Double LED indicator:<br>Red LED for 3V3 Power On<br>Green LED for user application<br>1 x 10/100Mbps Ethernet PHY interface<br>1 x 3V3 / 1A Supply (VOUT) from SODIMM-200 interface<br>1 x 3V SCL NAND chip for internal memory<br>1 x Positive overvoltage protection for VIN<br>1 x 32 kHz crystal for clock |

Table 3 On-board features



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## 3.3 IGEP™ COM AQUILA AM335x VARIANTS

The IGEP™ COM AQUILA AM335x modules are based in Texas Instruments Sitara AM335x Family (ARM Cortex-A8 processor). In the next figure are reflected the main differences of each model. The customized possibilities are collected in the chapter 2.4 (Page 8 -Ordering Information-).

Contact with sales@iseebcn.com for more information.

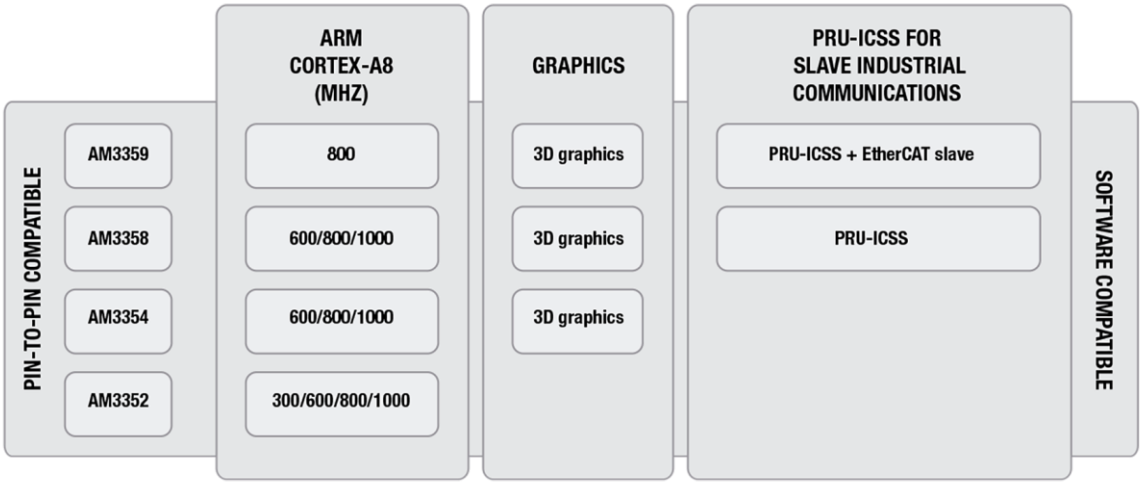


Figure 3 Texas Instruments™ AM335x Family Features

## 3.4 AM335x ARM CORTEX-A8 PROCESSORS

The AM335x, by Texas Instruments, are a family of highly integrated microprocessors based on the ARM Cortex-A8 processor. They have a high performance at low cost and are delivered with optional 3D graphics acceleration and key peripherals. They also include industrial options (such as EtherCAT and PROFIBUS) and support different high-level operating systems (Linux and Android).

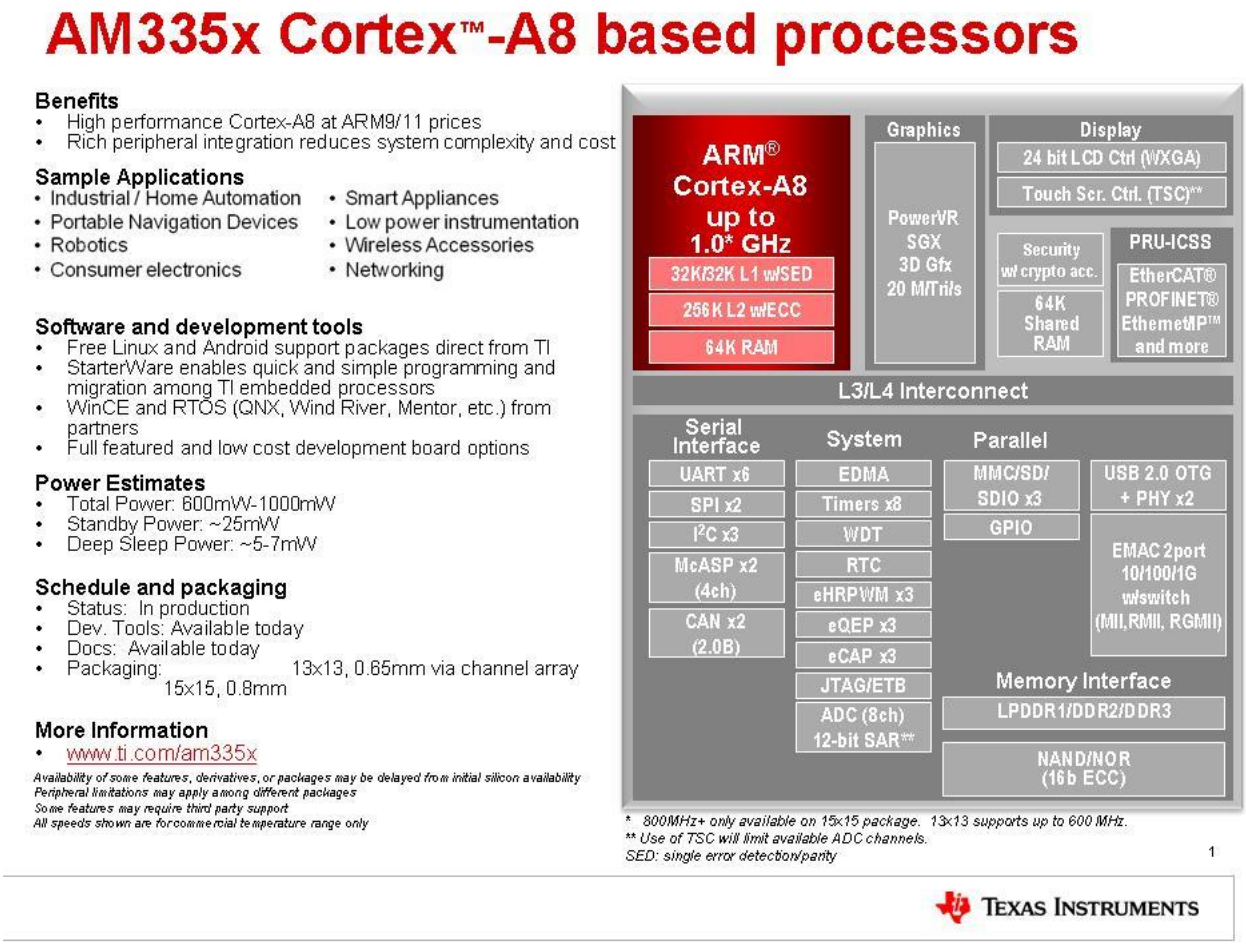


Figure 4 AM335x Processors Block Diagram

# 4 PRODUCT SPECIFICATION

## 4.1 IGEP™ COM AQUILA AM335x BLOCK DIAGRAM

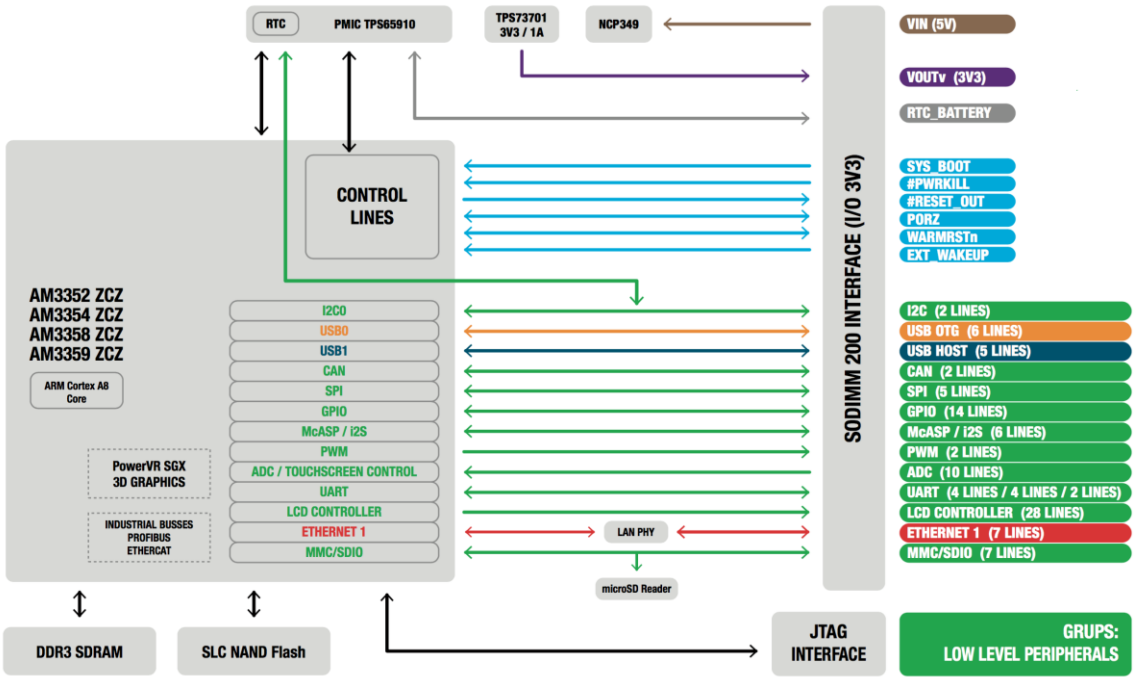


Figure 5 IGEP™ COM AQUILA AM335x Block Diagram

## 4.2 POWER SOURCES

### Supply Voltage

IGEP™ COM AQUILA AM335x module cannot be used as stand-alone module, so keep in mind that expansion board must power VIN signal input, this signal is defined into SODIMM-200 interface (from pin 1 to 4). VIN signal can vary from 3,8V to 5,5V DC, for more information see electrical characteristics table in Chapter 7.

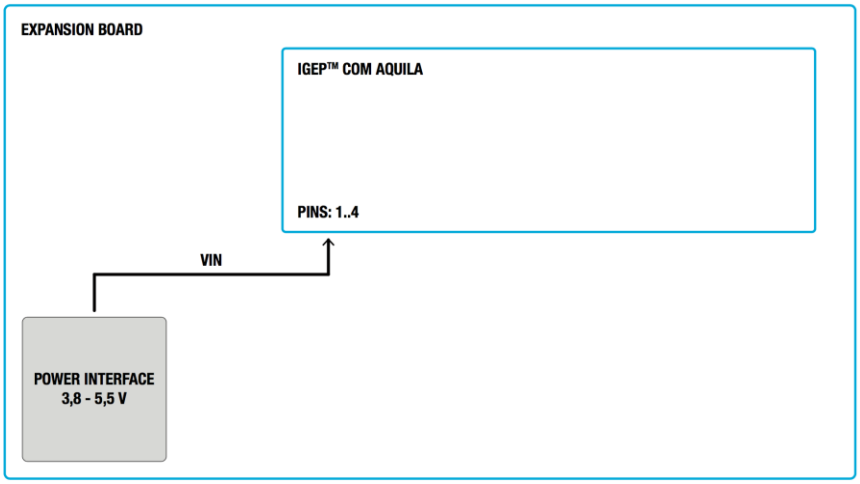


Figure 6 Power Supply Input Diagram

### Output Voltage and ADC Voltage reference

IGEP™ COM AQUILA AM335x module has a linear regulator that provides an output voltage 3,3 V @ 1 A (VOUT), VOUT signal is defined into SODIMM-200 interface from pin 5 to 7 and 9 to 12. If expansion board uses VOUT power supply, Hardware designer should take care to calculate VIN max current consumption.

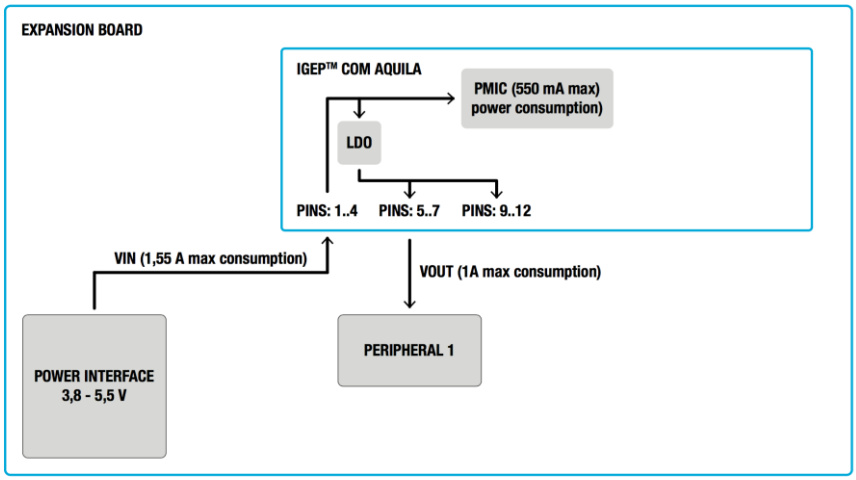


Figure 7 Power Supply Output Diagram

There is also available an output power reference supply (VREFP_ADC) of 1,8 V, defined into SODIMM-200 interface pin 184.It's used to fix the reference positive voltage for analog-to-digital converters (ADC).

## RTC Battery

The RTC_BATTERY signal (SODIMM-200 interface pin 13) allows to maintain RTC peripheral from IGEP™ COM AQUILA AM335x module when it is not power supplied (VIN). An example can be found into figure 8.

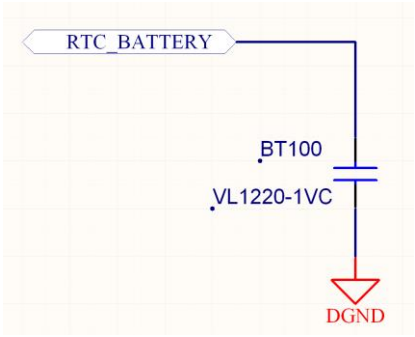


Figure 8 RTC Battery

## GND Pins

### Digital Ground

All the digital GND pins are internally connected together, so it's not need to connect all of them. However, the user has to considerer how many of them connect according the total consumption of the complete circuit (the IGEP™ COM Aquila AM335x and the base board developed). At the same time, to make the routing of buses easier, the ground connection chosen will be the nearest to the function used.

There have to be a minimum of 4 GND pins connected, distributed in the most possible equal way along the SODIMM-200 connector (to get an equalized ground).

### Analog Ground

AGND_ADC (SODIMM-200 interface pin 183) is a dedicated ground for IGEP™ COM AQUILA AM335x module analog converters. It improves analog captures avoiding the noise introduced by the logic ground when both grounds are detached.

### GND Earth

Hardware designer must take care of GND Earth.

In the figure 9 is an example about how to connect these grounds. The digital and analog grounds are separated by an EMI filter. By the other way, in order to enable GND Earth, R100 resistor must be unmounted and connect J991 to GND Earth source.

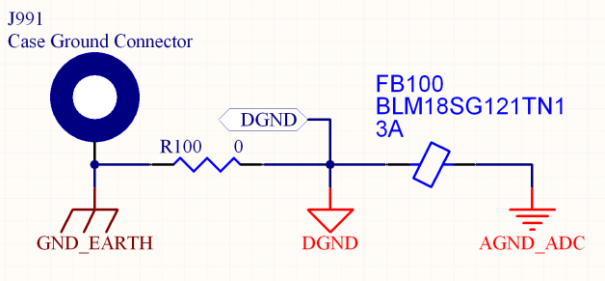


Figure 9 Ground Connections

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 5V INPUT POWER | | | | | | | |
| 1 | 5V | NA | VIN | NA | Power | Yes | Pins used to power up the module. Source voltage should be between 4V – 5.5V |
| 2 | 5V | NA | VIN | NA | Power | Yes | |
| 3 | 5V | NA | VIN | NA | Power | Yes | |
| 4 | 5V | NA | VIN | NA | Power | Yes | |
| 3V3 OUTPUT POWER | | | | | | | |
| 5 | 3V3 | NA | VOUT | NA | Power | Yes | Pins used as external 3V3@1A source voltage for a base board |
| 6 | 3V3 | NA | VOUT | NA | Power | Yes | |
| 7 | 3V3 | NA | VOUT | NA | Power | Yes | |
| 9 | 3V3 | NA | VOUT | NA | Power | Yes | |
| 10 | 3V3 | NA | VOUT | NA | Power | Yes | |
| 11 | 3V3 | NA | VOUT | NA | Power | Yes | |
| 12 | 3V3 | NA | VOUT | NA | Power | Yes | |
| RTC BATTERY | | | | | | | |
| 13 | VBAT | NA | RTC_BATTERY | NA | Power | Yes | RTC battery positive pin. Battery or capacitor limit voltage should be: 2V52; 3V; 3V15 and VIN |
| 1V8 OUTPUT POWER | | | | | | | |
| 184 | 1V8 | D8 | VREFP_ADC | NA | Power | Yes | Supply voltage range for ADCs |
| DIGITAL GROUND | | | | | | | |
| 18 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 26 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 32 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 39 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 50 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 58 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 71 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 82 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 88 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 94 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 102 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 111 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 116 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 129 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 142 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 147 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 160 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 171 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| 200 | GND | NA | DGND | NA | Power | Yes | Digital Ground |
| ANALOG GROUND | | | | | | | |
| 183 | GND | E8 | VSSA_ADC | NA | Power | Yes | Analog Ground for ADCs |

Table 4 Power Sources pins

## 4.3 CONTROL SIGNALS

There are different pins used as general control signals. They affect: Boot Mode, management of the power supply, resets and wake up the system from a state of suspension.

### Boot Mode

The Boot mode functionality (SODIMM-200 interface pin 8) is equivalent to #SYS_BOOT4 (SYS_BOOT4 inverted) signal. When IGEP™ COM AQUILA AM335x module is powered on, it reads this pin and it boots from NAND/MMC0 or MMC0 in function of its status, the following table shows the complete sequence.

| Pin #8 | Boot Mode |
|---|---|
| NC | Sequence: UART0 ➔ SPI0 ➔ XIP ➔ MMC0 |
| DGNG | Sequence: NAND ➔ NANDI2C ➔ MMC0 ➔ UART0 |

Table 5 Boot Mode pin

#SYS_BOOT4 pin uses LCD_DATA4 signal (SODIMM-200 interface pin 141) to control sysboot mode. Hardware designer can use independently LCD_DATA4 and #SYS_BOOT4 signals because there are isolated.

It's recommended to use a jumper header or a switch in series with a low resistor value (as a short circuit protector element) tied to GND into expansion board.

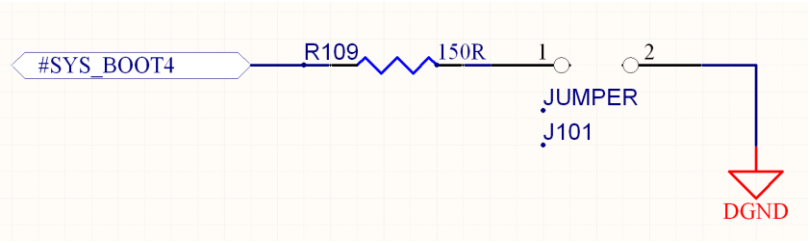


Figure 10 Boot Mode: Jumper Selector

## Reset pins

There are three different Reset-IOs: #PWR_KILL (SODIMM-200 interface pin 14), PORZ (SODIMM-200 interface pin 16) and WarmResetn (SODIMM-200 interface pin 17):

If #PwrKill is driven to Low state (default timeout 8 seconds), power supplies from PMIC will be turned off until #PwrKill is set High. The following diagram shows #PwrKill distribution.

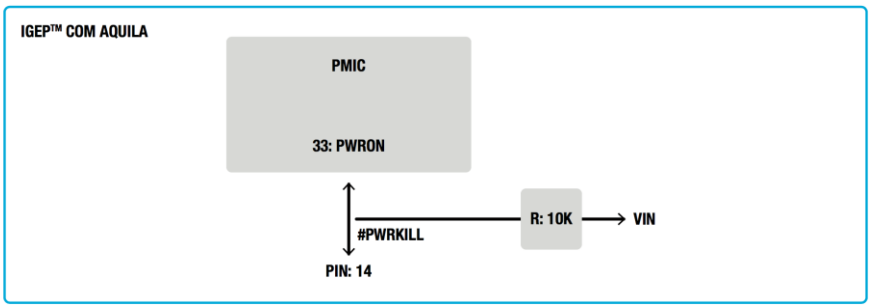


Figure 11 PowerKill Reset

If PORz is driven to Low state (at least 154 microseconds), Power-On-Reset (PORz) will be active and will reset the complete processor and all the logic that uses asynchronous reset. The following diagram shows PORz distribution.

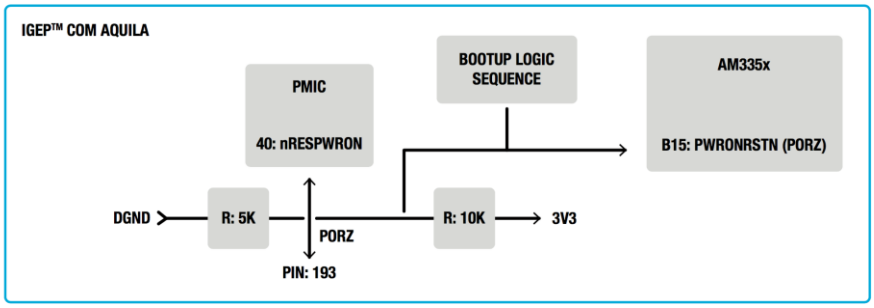


Figure 12 PORz – Power-On-Reset

If WarmResetn is driven to Low state (at least 90 nanoseconds), Warm Reset is active and reset partially the processor: the SYSBOOT pins are not latched, PLLs are not affected and most debug subsystem logic is not affected (this allows to maintain any debug session throughout a warm reset event). As an input, it's typically used by an external source as a device reset and as an output, it can be used to reset external devices. The following diagram shows WarmResetn distribution.

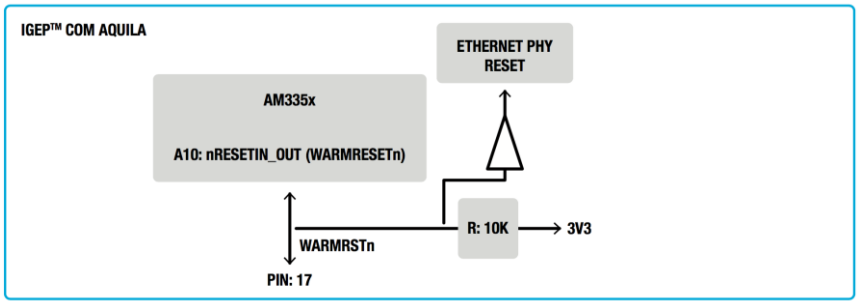


Figure 13 WarmReset

Moreover, there is a generic output reset signal (SODIMM-200 interface pin 15) controlled through of GPIO3_8. This reset doesn't affect to processor and it is intended to use for external peripherals. The following diagram shows #RESET_OUT distribution.

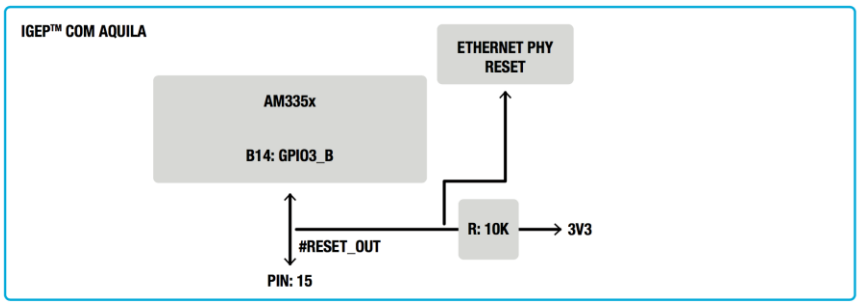


Figure 14 Reset Out

## External Wake Up

The last control signal is a Wake Up input (SODIMM-200 interface pin 193). EXT_WAKEUP is used to recover the processor from a state of suspension. The following diagram shows EXT_WAKEUP distribution.

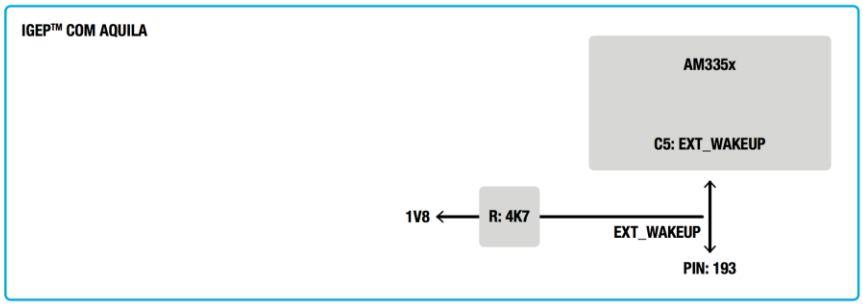


Figure 15 Wake Up Input

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 8 | 3V3 | T1 | #SYS_BOOT4 | 0 | IN | Yes | SYS_BOOT4 signal inverted. Sequence should be:<br>NC: UART0 – SPI0 – XIP – MMC0<br>GND: NAND – NAND_I2C – MMC0 – UART0 |
| | | | | | | | |
| 14 | 5V | NA | #PWRKILL | NA | IO | Yes | Tied to GND to cut off power sources from PMIC |
| 15 | 3V3 | B14 | #RESET_OUT | 7 | OUT | Yes | This pin is used as external reset source for a base board.<br>Active Low |
| 16 | 3V3 | B15 | PORZ | 0 | IO | Yes | Power ON Reset. Active Low. |
| 17 | 3V3 | A10 | WARMRSTn | 0 | IO | Yes | Warm Reset. Active Low. |
| 193 | 1V8 | C5 | EXT_WAKEUP | 0 | IN | Yes | EXT_WAKEUP input |

Table 6 Control Signal pins

## 4.4 ETHERNET

The module can be connected to a standard 10 or 100 Mbps Ethernet system. For this function, there is a block of pins in the SODIMM-200 that can be connected directly to the Ethernet LAN. Both transmission and reception lines (TX and RX) are differential (in the pin function is indicated the Negative and Positive) and they should be connected to isolation magnetics. The data lines have to be equal length and symmetric, and respect a 100Ω differential impedance in the layout traces. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

Moreover, the magnetics module has a critical effect so it has to be designed carefully. In order to obtain a smaller size, it's usual to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they have to respect a separation under of 25mm between them and the RJ45 connector, and 20mm or greater between them and the SODIMM-200 connector.

There are also two outputs to manage LEDs. These LEDs are used to indicate the good functioning of the Ethernet connection. The first one (output #ETN_LED2, usually a yellow LED) gives an indication about the line speed (LED off for 10Mbps and LED on for 100Mbps). The other (output #ETN_LED1, usually a green LED) gives an indication about the line activity: LED on indicates a valid link; when LED is blinking there is data traffic.

In the next figure is shown an example of connection diagram, using a RJ45 jack with integrated magnetics.

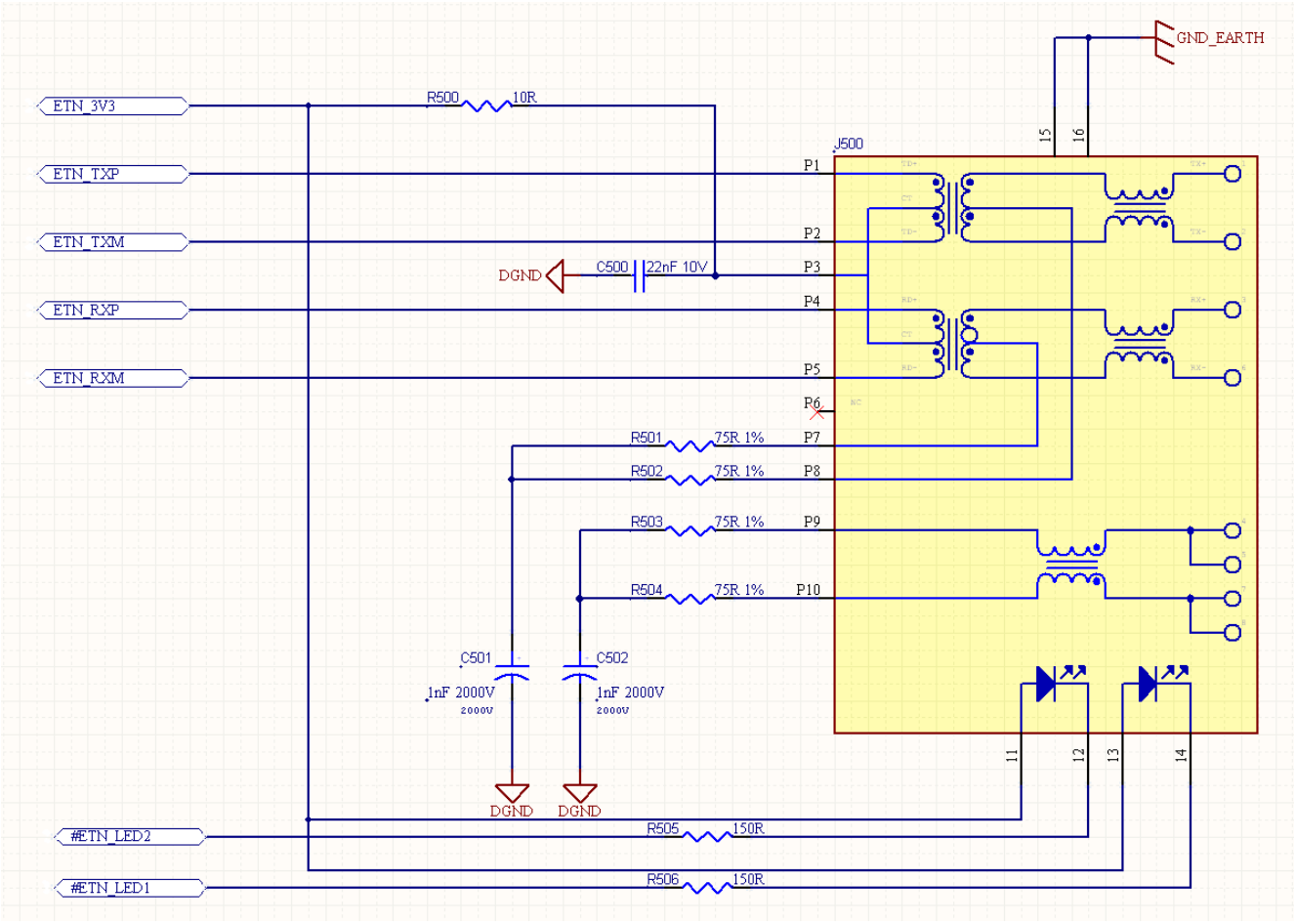


Figure 16 Ethernet standard circuit

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 19 | DIF | NA | ETN_TXN | NA | ETH | Yes | Analog Transmit Data Negative. Differential output to magnetics |
| 20 | 3V3 | NA | #ETN_LED2 | NA | OUT | Yes | Active Low. LED2 Yellow means 100Mbps speed. Inactive if 10Mbps. Line isolated through a driver. |
| 21 | DIF | NA | ETN_TXP | NA | ETH | Yes | Analog Transmit Data Positive. Differential output to magnetics |
| 22 | 3V3 | NA | ETN_3V3 | NA | Power | Yes | 3V3 to magnetics |
| 23 | DIF | NA | ETN_RXM | NA | ETH | Yes | Analog Receive Data Negative. Differential output to magnetics |
| 24 | 3V3 | NA | #ETN_LED1 | NA | OUT | Yes | Active Low. LED1 Green indicates valid link and blinks when there is activity. Line isolated through a driver. |
| 25 | DIF | NA | ETN_RXP | NA | ETH | Yes | Analog Receive Data Positive. Differential output to magnetics. |

Table 7 Ethernet pins

## 4.5 USB CONNECTIONS

There are two possibilities to connect the module to other USB devices: with a standard Host base and with an OTG (On-The-Go) interface.

The USB 2.0 Host connection is provided for connecting other devices acting as Clients of the module (for example, an external HDD). The SODIMM-200 connector lines referred to this function are adapted for a USB type A receptacle (see wiring example in the next figure).

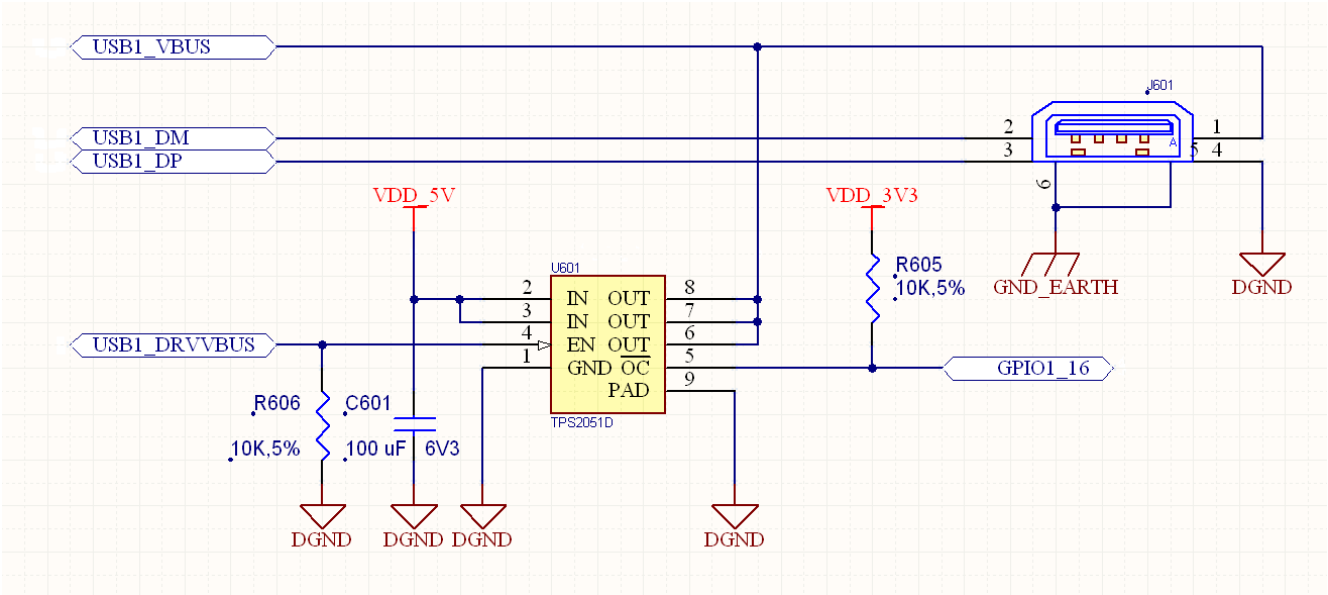


Figure 17 USB 2.0 Host connections

The USB 2.0 OTG connection allows the configuration of the board as Host or Client in function of the wire of connection used for linking both devices (the IGEP™ module and the external device; adapting the SODIMM-200 connector lines for an USB type AB). It's defined by the pin #33 (ID): when the board detects this pin connected at ground, it will be an A-device; by the other side, if the pin is floating (NC) it will be a B-device.

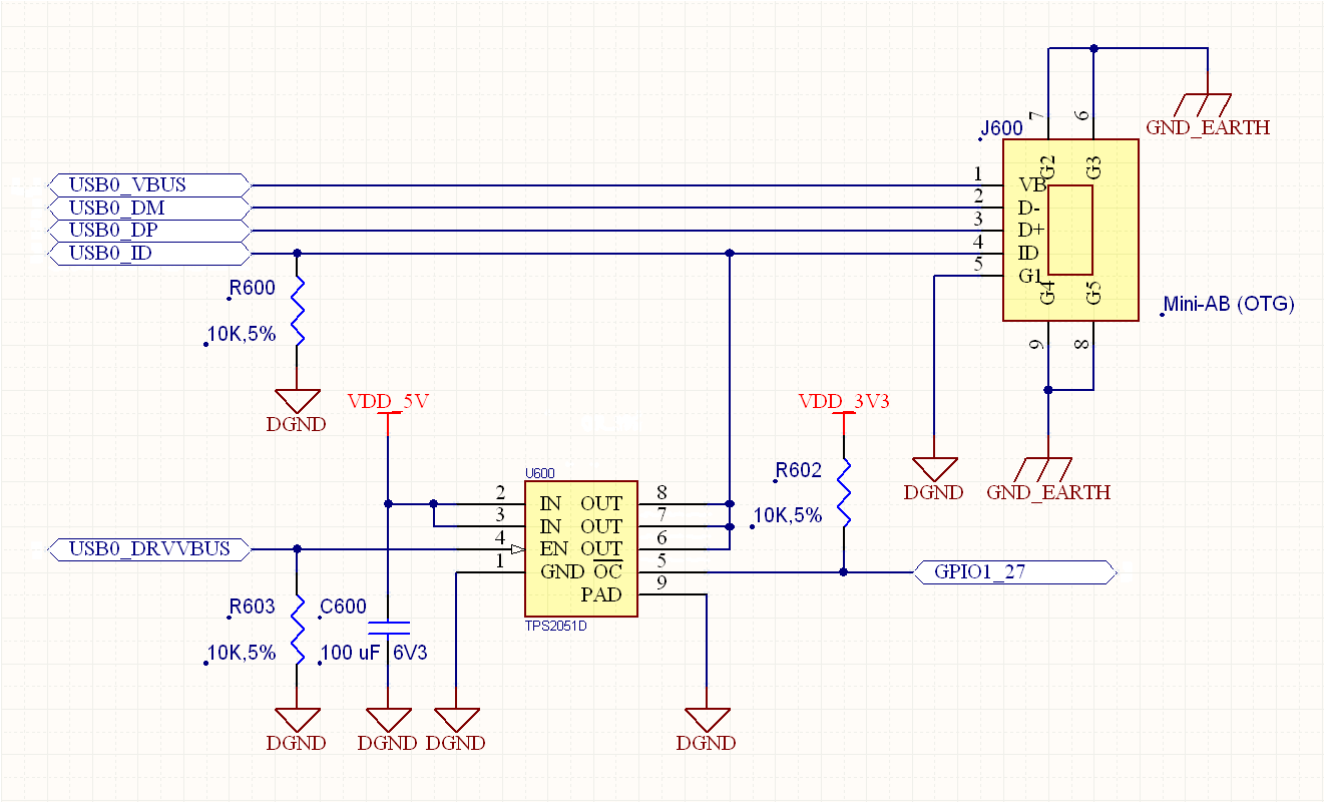


Figure 18 MiniUSB AB 2.0 OTG connections

The GPIO1_26 and GPIO1_27 are, in both cases, optional pins used to detect if there has been an over-consumption (for example a short-circuit). Although in the examples are used this references, it's possible to apply any other of the free GPIO pins if the user wants to implement this feature.

It must be respected a 90Ω (+/-15%) differential impedance in the layout traces when the base board will be designed. At the same time, the traces have to be equal length and symmetric, with regards of shape, length and via count. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

To protect the VBUS against overcurrent, the USB power source current have to be less or equal than 500mA, and the user must to provide a protection in the base board as it is showed into Figure 8 and Figure 9 examples. The IGEP™ COM AQUILA AM335x includes into each USB peripheral Transient voltage suppressors and Common mode filters.

The following table offers the list in the SODIMM-200 of the pins related with both of USB connections.

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| USB HOST | | | | | | | |
| 27 | 3V3 | F15 | USB1_DRVVBUS | 0 | OUT | Yes | Active High. Enables external VBUS power supply |
| 28 | 3V3 | R13 | GPIO1_16 | 7 | IN | No | #USB1_OC: Active Low. Over current indication to module. It could be another GPIO from processor. |
| 29 | DIF | R18 | USB1_DM | 0 | USB | Yes | Analog D- data pin of the USB cable |
| 30 | 5V | T18 | USB1_VBUS | 0 | Power | Yes | VBUS pin of the USB cable |
| 31 | DIF | R17 | USB1_DP | 0 | USB | Yes | Analog D+ data pin of the USB cable |
| USB OTG | | | | | | | |
| 33 | ANALOG | P16 | USB0_ID | 0 | USB | Yes | ID pin of the USB cable. A-device is gounded; B-device is floating |
| 34 | 3V3 | F16 | USB0_DRVVBUS | 0 | OUT | Yes | Active High. Enables external VBUS power supply |
| 35 | DIF | N18 | USB0_DM | 0 | USB | Yes | Analog D- data pin of the USB cable |
| 36 | 3V3 | V17 | GPIO1_27 | 7 | IN | No | #USB0_OC: Active Low. Over current indication to module. It could be another GPIO from processor. |
| 37 | DIF | N17 | USB0_DP | 0 | USB | Yes | Analog D+ data pin of the USB cable |
| 38 | 5V | P15 | USB0_VBUS | 0 | Power | Yes | VBUS pin of the USB cable |

Table 8 USB pins

## 4.6 I2C: Inter-Integrated Circuit Interface

The IGEP™ COM AQUILA AM335x module can be connected to other peripheral devices by the I2C serial bus. There are two pins in the SODIMM-200 that may be used for this application: The I2C0 data line and the I2C0 bus clock.

The IGEP COM AQUILA AM335x uses a 3V3 voltage levels for I2C buses. In some cases, bidirectional voltage translators should be necessary to adapt voltage levels between ICs.

In the next example, it has been connected an EEPROM to the IGEP COM AQUILA AM335x using the I2C interface.

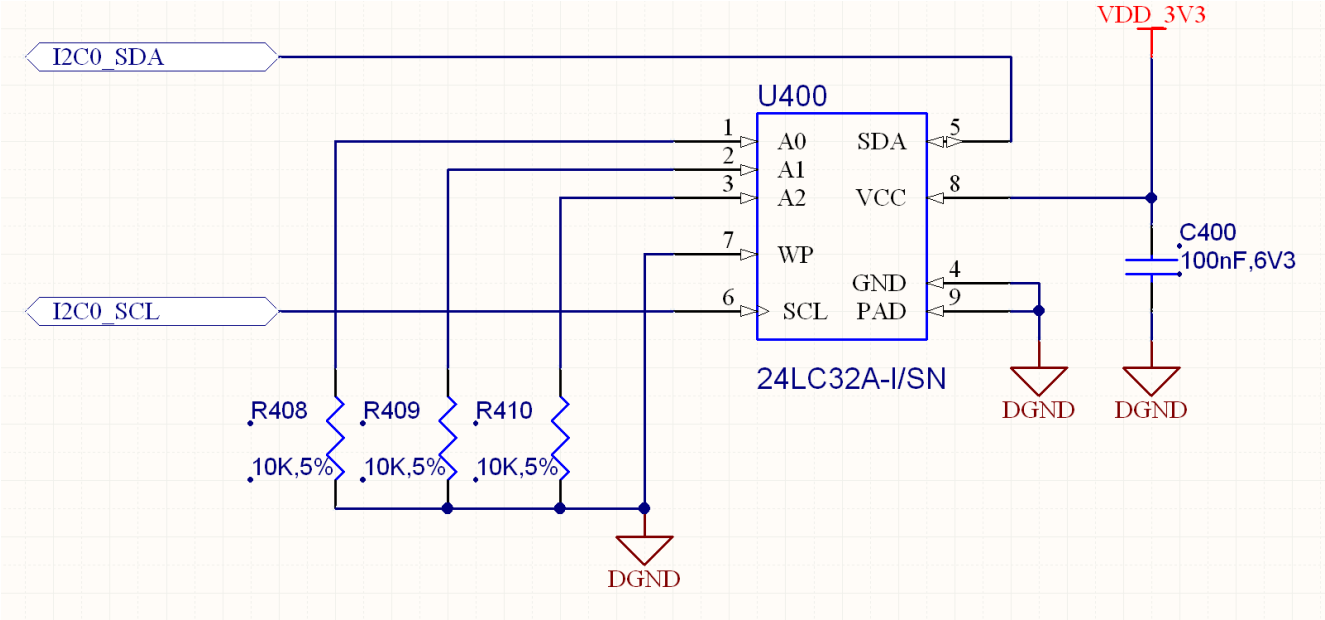


Figure 19 I2C example: EEPROM connection

If the user needs to use another I2C peripheral from another SODIMM-200 pins, it is necessary to add a 5K pull up resistors to data and clock lines.

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 40 | 3V3 | C17 | I2C0_SDA | 0 | IO | Yes | I2C0 bus data. 0x2D is used by IGEP COM Aquila. This signal has a 5K PU resistor |
| 41 | 3V3 | C16 | I2C0_SCL | 0 | IO | Yes | I2C0 bus clock. This signal has a 5K PU resistor |

Table 9 I2C pins

## 4.7 PWM: Pulse-Width Modulation

If it's needed a control over other devices via a Pulse-Width Modulation (PWM), the module offers a PWM peripheral with 16 bits time-base with Period and Frequency control and two outputs.

If system frequency = SYSCLKOUT = 100MHz, that is, CPU clock. TBCLK = SYSCLKOUT (preescaler is set to x1), minimum PWM frequency is 1525 Hz (16 bits duty cycle resolution) and max PWM frequency is 5 MHz (4 bits duty cycle resolution). More information at chapter 15.2 from AM335x Technical Reference Manual.

In the next figure is shown a simple example in which is sent the PWM signal to a RC-filter.

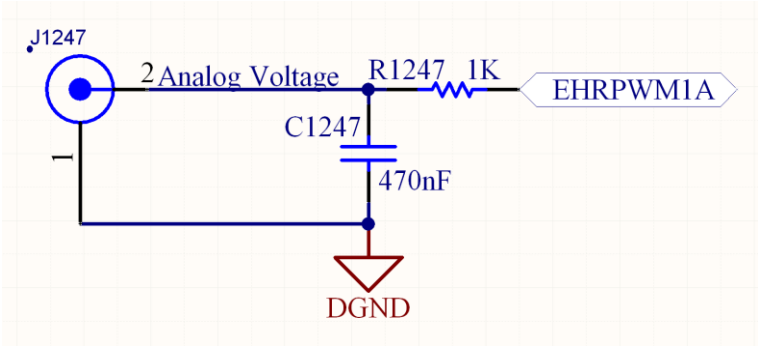


Figure 20 PWM example: RC filter

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 149 | 3V3 | U14 | EHRPWM1A | 6 | OUT | No | eHRPWM1 A output |
| 150 | 3V3 | T14 | EHRPWM1B | 6 | OUT | No | eHRPWM1 B output |

Table 10 PWM pins

## 4.8 SPI: Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is one more of the different possibilities to connect the module to external peripherals. It's a full duplex synchronous bus, supporting a single master and up to two slave devices each SPI peripheral.

The IGEP™ COM AQUILA AM335x uses a 3V3 voltage levels for SPI buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs.

In the next figure is an example to connect the IGEP™ COM AQUILA AM335x module to an accelerometer via the Serial Peripheral Interface.

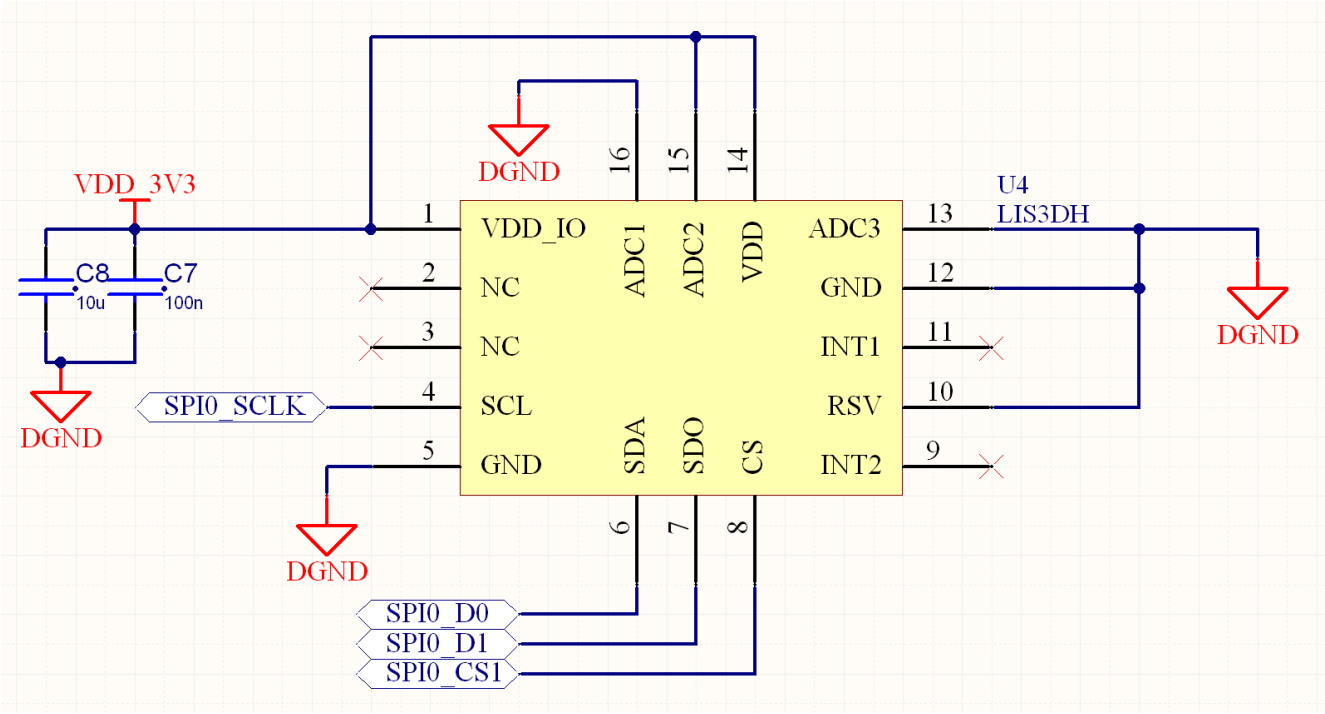


Figure 21 SPI example: accelerometer circuit

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 44 | 3V3 | A16 | SPI0_CS0 | 0 | OUT | No | SPI0 Slave chip select 0 signal |
| 45 | 3V3 | C15 | SPI0_CS1 | 0 | OUT | No | SPI0 Slave chip select 1 signal |
| 46 | 3V3 | B17 | SPI0_D0 | 0 | OUT | No | SPI0 Master Output-Slave Input (MOSI) |
| 47 | 3V3 | B16 | SPI0_D1 | 0 | IN | No | SPI0 Master Input-Slave Output (MISO) |
| 48 | 3V3 | A17 | SPI0_SCLK | 0 | OUT | No | SPI0 Clock |

Table 11 SPI pins



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## 4.9 MMC: Multi Media Card Interface

The IGEP™ COM AQUILA AM335x has two MMC (Multi Media Card) interfaces. The first one (MMC0) is used into on-board bootable uSD card reader socket. The user also has available a second interface (MMC1) into SODIMM-200 connector.

The module has installed in the board its own SD-Card reader and it's used to boot and check its global function when it's tested in factory.

The second interface (MMC1), which can be configured for other applications (in example, to expand memory capacities or used as a backup memory), is not available as a boot up device due *Boot Mode* configuration.

The next example shows how to connect a uSD card reader to MMC1, using a 10k pull-up resistor tied to 3V3 in the lines SD1_Dx, SD1_CD and SD1_CLK. Optionally, it's possible to use 10R series resistor in the same lines to avoid overshoot issues.

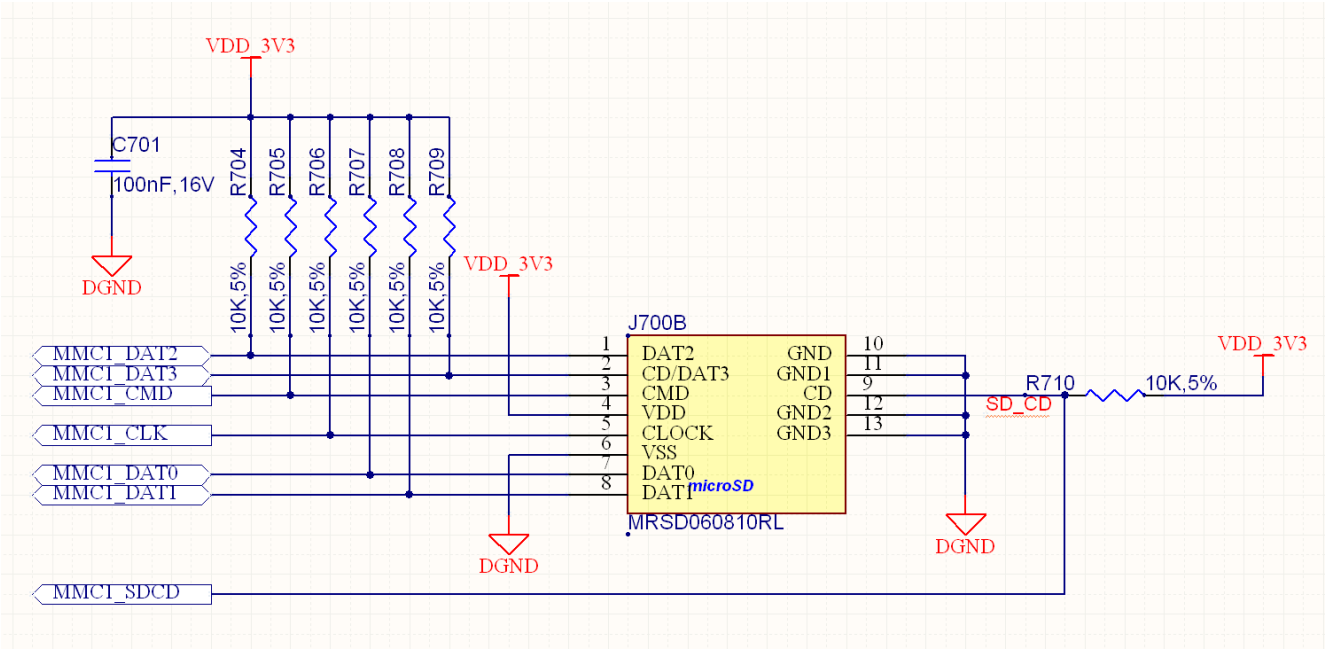


Figure 22 MMC example: uSD card reader

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 51 | 3V3 | B13 | MMC1_SDCD | 4 | IN | No | SD Card Detect for MMC1. There are no components between this pin and AM335x ball |
| 52 | 3V3 | K18 | MMC1_DAT0 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 0. There are no components between this pin and AM335x ball |
| 53 | 3V3 | L18 | MMC1_DAT1 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 1. There are no components between this pin and AM335x ball |
| 54 | 3V3 | L17 | MMC1_DAT2 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 2. There are no components between this pin and AM335x ball |
| 55 | 3V3 | L16 | MMC1_DAT3 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 3. There are no components between this pin and AM335x ball |
| 56 | 3V3 | V9 | MMC1_CMD | 2 | IO | No | MMC/SD/SDIO 1 Command. There are no components between this pin and AM335x ball |
| 57 | 3V3 | U9 | MMC1_CLK | 2 | IO | No | MMC/SD/SDIO 1 Clock. There are no components between this pin and AM335x ball |

Table 12 MMC pins

## 4.10 UART: Universal Asynchronous Receiver-Transmitter

There are three defined UART devices in the module in order to control serial devices or debug via serial. They are available in the SODIMM-200 in three blocks of pins.

The IGEP™ COM AQUILA AM335x uses a 3V3 voltage levels for UART buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs.

The IGEP™ COM AQUILA AM335x uses UART0 as a Kernel Debug Peripheral. This UART is an inexpensive method to detect and repair system issues. It's advisable to use another UART instead of UART0 to preserve this functionality. In the next figure is shown how to connect the UART0 to a popular serial debug connector (for example: TTL-232R-3V3).

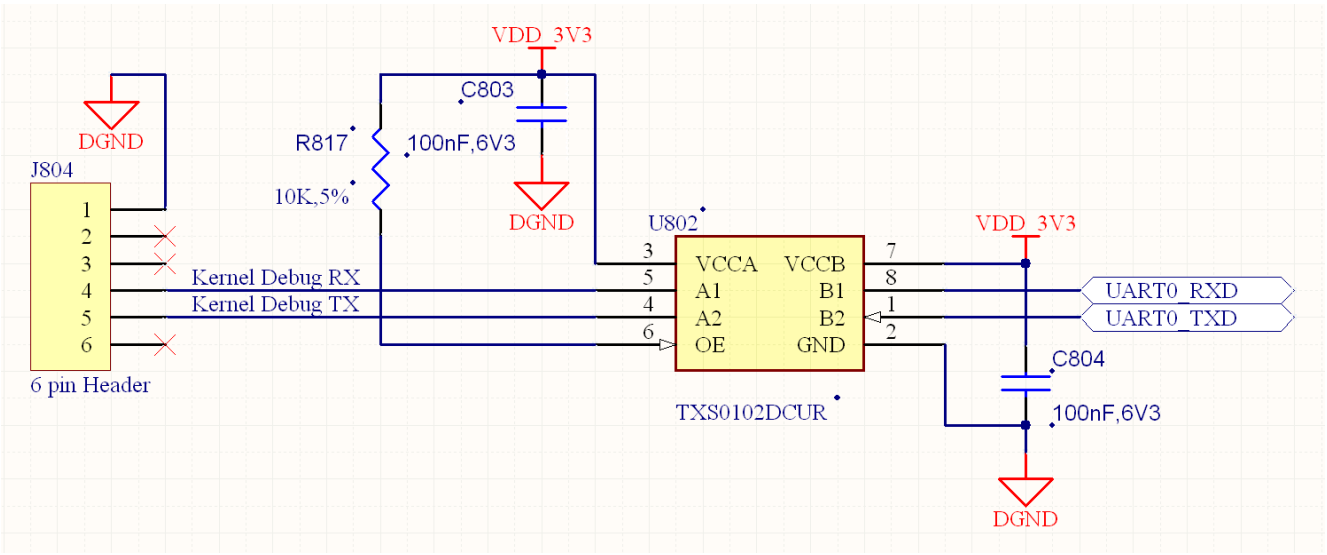


Figure 23 UART0 Debug connections

In the next figure is shown another example to use the UART1 as RS485 bus.

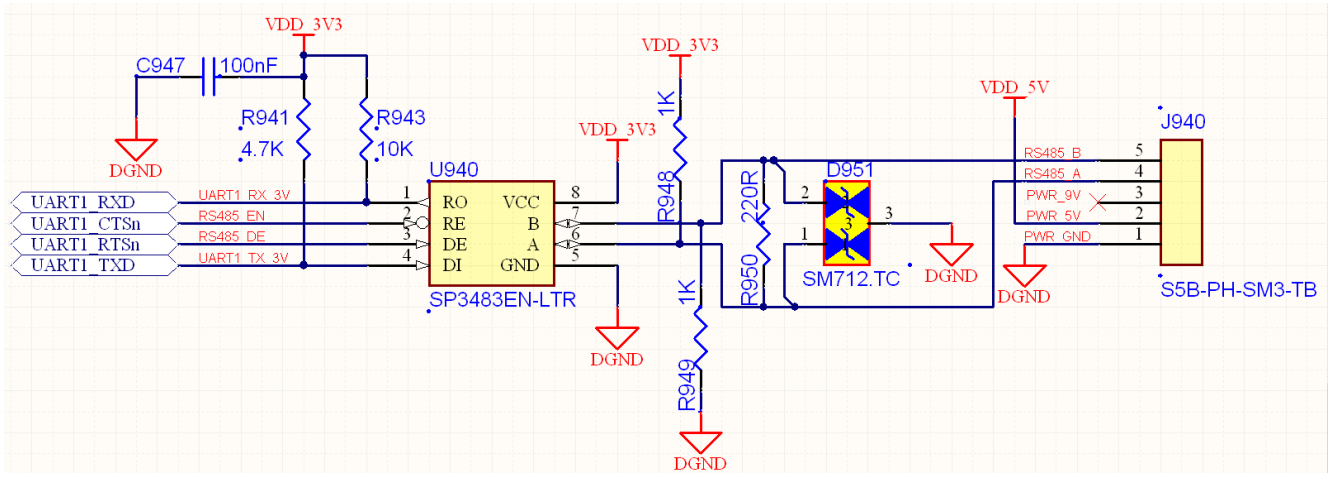


Figure 24 RS485 example: RS485 circuit

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 1ST UART | | | | | | | |
| 59 | 3V3 | E16 | UART0_TXD | 0 | OUT | No | Debug UART0 Transmit Data Output |
| 60 | 3V3 | E15 | UART0_RXD | 0 | IN | No | Debug UART0 Receive Data Input |
| 61 | 3V3 | E18 | UART0_CTSn | 0 | IN | No | UART0 CTSn Input |
| 62 | 3V3 | E17 | UART0_RTSn | 0 | OUT | No | UART0 RTSn Output |
| 2ND UART | | | | | | | |
| 63 | 3V3 | D15 | UART1_TXD | 0 | OUT | No | UART1 Transmit Data Output |
| 64 | 3V3 | D16 | UART1_RXD | 0 | IN | No | UART1 Receive Data Input |
| 65 | 3V3 | D18 | UART1_CTSn | 0 | IN | No | UART1 CTSn Input |
| 66 | 3V3 | D17 | UART1_RTSn | 0 | OUT | No | UART1 RTSn Output |
| 3RD UART | | | | | | | |
| 67 | 3V3 | J17 | UART5_TXD | 3 | OUT | No | UART5 Transmit Data Output |
| 68 | 3V3 | H16 | UART5_RXD | 3 | IN | No | UART5 Receive Data Input |

Table 13 UART pins

## 4.11 CAN BUS: Controller Area Network

The module can be integrated in a global system using the serial standard CAN Bus. The CAN Bus is a standard designed to allow microcontrollers and devices to communicate with each other without a host computer. It's a differential half duplex data bus, using shielded or unshielded twisted differential pair wiring, with an impedance termination of 120Ω at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion.

A CAN Transceiver is needed on the baseboard to connect the system to the CAN Bus. In the next example, are showing this application using the MCP2551 chip (it's a high-speed CAN Transceiver).

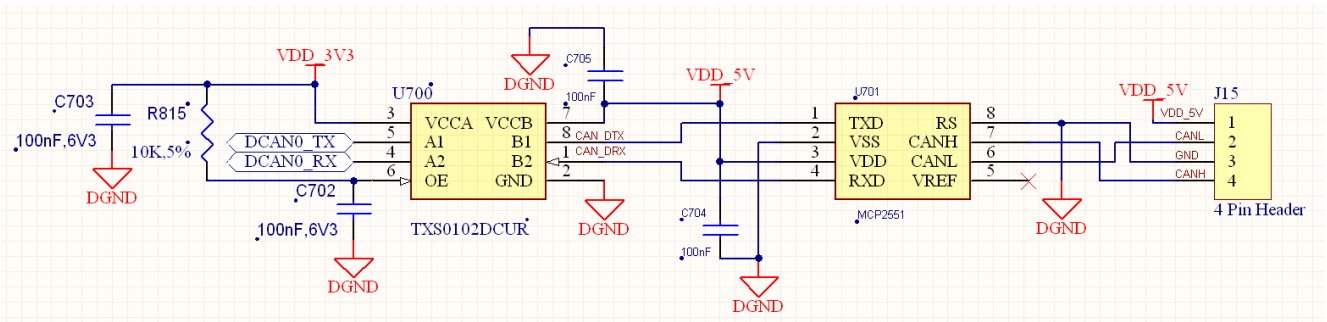


Figure 25 CAN Bus circuit example

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 76 | 3V3 | J18 | DCANo_TX | 1 | OUT | No | CANo Transmission line |
| 81 | 3V3 | K15 | DCANo_RX | 1 | IN | No | CANo Reception line |

Table 14 CAN pins

## 4.12 I2S: Serial Audio Port

It's also available a MCASP transceiver. It's a digital multichannel audio serial port used by microprocessors, DSPs and popular industry audio CODECs that implement the inter-IC sound bus standard (I2S).

In the next example is connected a Stereo CODEC with Headphone AMP to the Serial Audio Port in the IGEP™ COM AQUILA AM335x module.

DEV_SLP register of the PMIC must be at 0 to use the pin MCASP0_CLKX. Default firmware allows to use this functionality. For more information, refer to Texas Instruments TPS65910 manual.

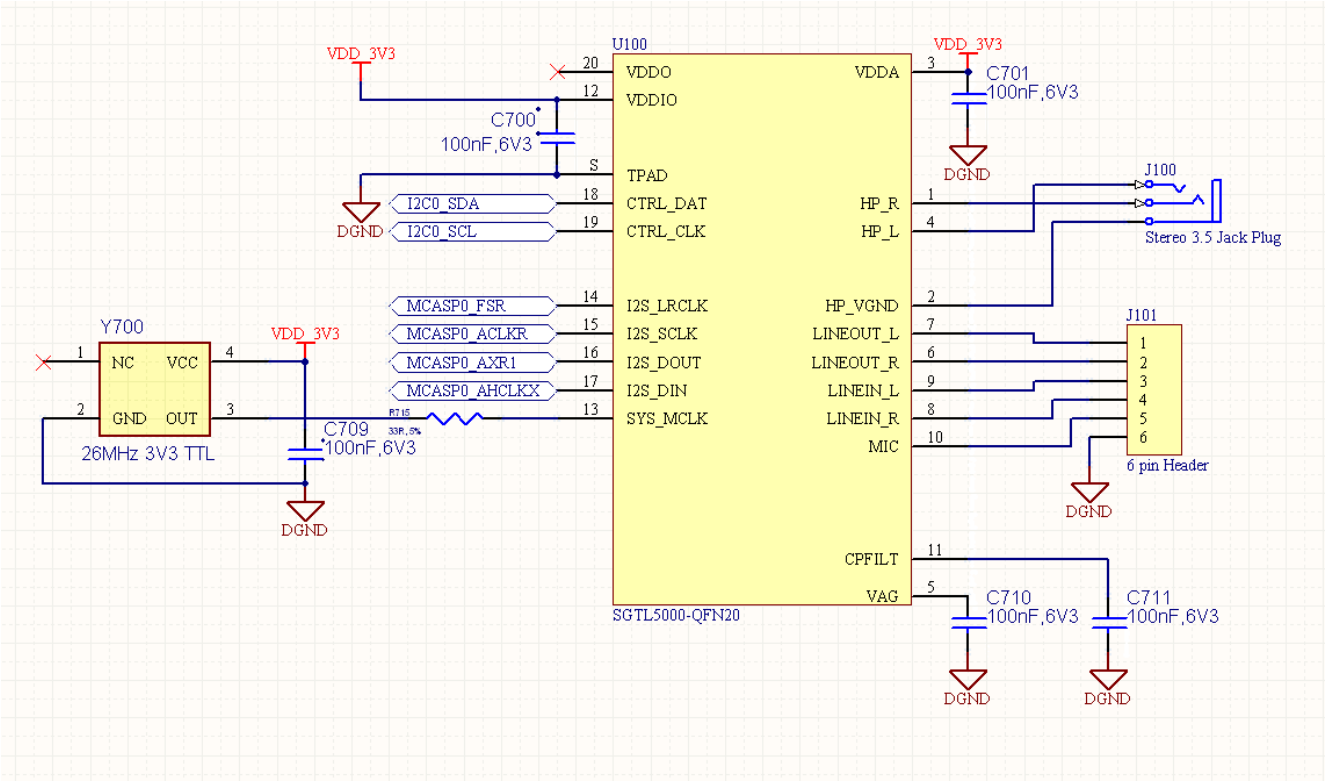


Figure 26 I2S example: Stereo CODEC with Headphone AMP

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 83 | 3V3 | D12 | MCASP0_AXR0 | 0 | IO | No | McASP0 Serial Data (IN/OUT) 0 |
| 84 | 3V3 | D13 | MCASP0_AXR1 | 0 | IO | No | McASP0 Serial Data (IN/OUT) 1 |
| 85 | 3V3 | A14 | MCASP0_AHCLKX | 0 | IO | No | McASP0 Transmit Master Clock |
| 86 | 3V3 | B12 | MCASP0_ACLKR | 0 | IO | No | McASP0 Receive Bit Clock |
| 87 | 3V3 | C13 | MCASP0_FSR | 0 | IO | No | McASP0 Receive Frame Sync |
| 158 | 3V3 | V16 | McASP0_ACLKX | 6 | IO | No | McASP0 Transmit Bit Clock |

Table 15 McASP (I2S) pins



NIF:ESB64377005 Document: **MAN-PR-IGEP0033-RBxx-002** / Revision: **3.0** / Date: **27/06/2015**

## 4.13 LCD CONTROLLER

There is a set of pins in the SODIMM-200 connector used as the parallel data bus to control a LCD screen used by the user.

Common mode capacitors could be added (optionally) between video data lines and GND for high frequency noise attenuation. Typical capacitance values should be between 22pF and 47pF.

Low resistance capacitors should be necessary to protect overshoot voltage. It can be solved using a 10R series resistor to data and clock lines.

In the next page is an example of circuit to get a LCD to HDMI interface.

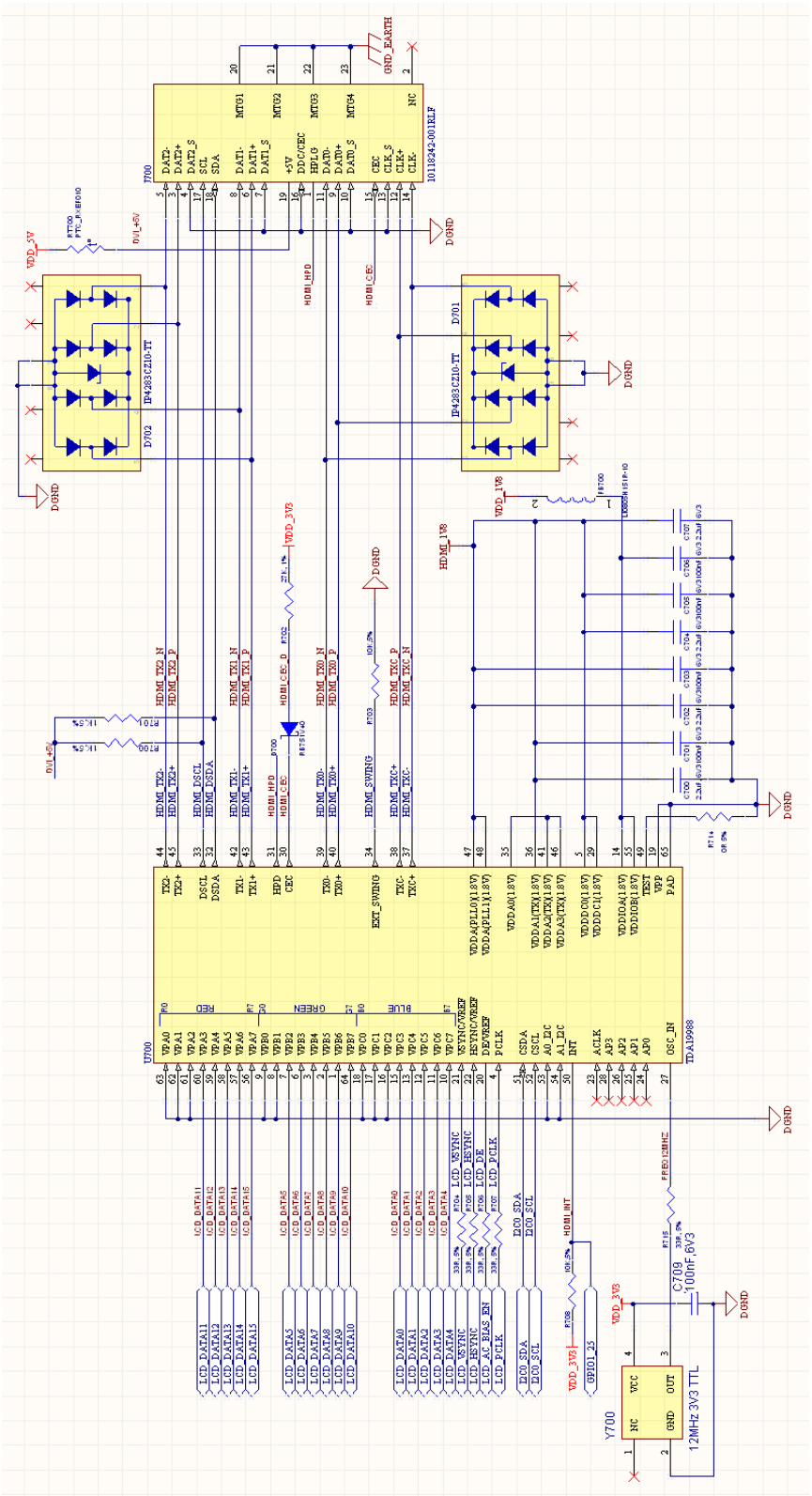

Figure 27 LCD Full-HD HDMI circuit example

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 117 | 3V3 | U10 | LCD_DATA23 | 1 | OUT | No | LCD data bus |
| 118 | 3V3 | U12 | LCD_DATA20 | 1 | OUT | No | LCD data bus |
| 119 | 3V3 | V13 | LCD_DATA17 | 1 | OUT | No | LCD data bus |
| 120 | 3V3 | U4 | LCD_DATA11 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 121 | 3V3 | V2 | LCD_DATA12 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 122 | 3V3 | V3 | LCD_DATA13 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 123 | 3V3 | V4 | LCD_DATA14 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 124 | 3V3 | T5 | LCD_DATA15 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 125 | 3V3 | T10 | LCD_DATA22 | 1 | OUT | No | LCD data bus |
| 126 | 3V3 | T12 | LCD_DATA19 | 1 | OUT | No | LCD data bus |
| 127 | 3V3 | T2 | LCD_DATA5 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 128 | 3V3 | T3 | LCD_DATA6 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 130 | 3V3 | T4 | LCD_DATA7 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 131 | 3V3 | U1 | LCD_DATA8 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 132 | 3V3 | U2 | LCD_DATA9 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 133 | 3V3 | U3 | LCD_DATA10 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 134 | 3V3 | T11 | LCD_DATA21 | 1 | OUT | No | LCD data bus |
| 135 | 3V3 | R12 | LCD_DATA18 | 1 | OUT | No | LCD data bus |
| 136 | 3V3 | U13 | LCD_DATA16 | 1 | OUT | No | LCD data bus |
| 137 | 3V3 | R1 | LCD_DATA0 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 138 | 3V3 | R2 | LCD_DATA1 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 139 | 3V3 | R3 | LCD_DATA2 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 140 | 3V3 | R4 | LCD_DATA3 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 141 | 3V3 | T1 | LCD_DATA4 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 143 | 3V3 | R5 | LCD_HSYNC | 0 | OUT | No | LCD Horizontal Sync |
| 144 | 3V3 | U5 | LCD_VSYNC | 0 | OUT | No | LCD Vertical Sync |
| 145 | 3V3 | R6 | LCD_AC_BIAS_EN | 0 | OUT | No | LCD AC bias enable chip select |
| 146 | 3V3 | V5 | LCD_PCLK | 0 | OUT | No | LCD pixel clock |

Table 16 LCD pins

## 4.14 GPIO: General Purpose Input Output

GPIOs are input/output (IO) general purpose pins used to control LEDs, relays, switch, etc. In the next figure is shown a basic circuit with an input pushbutton and two outputs to manage LED signals.

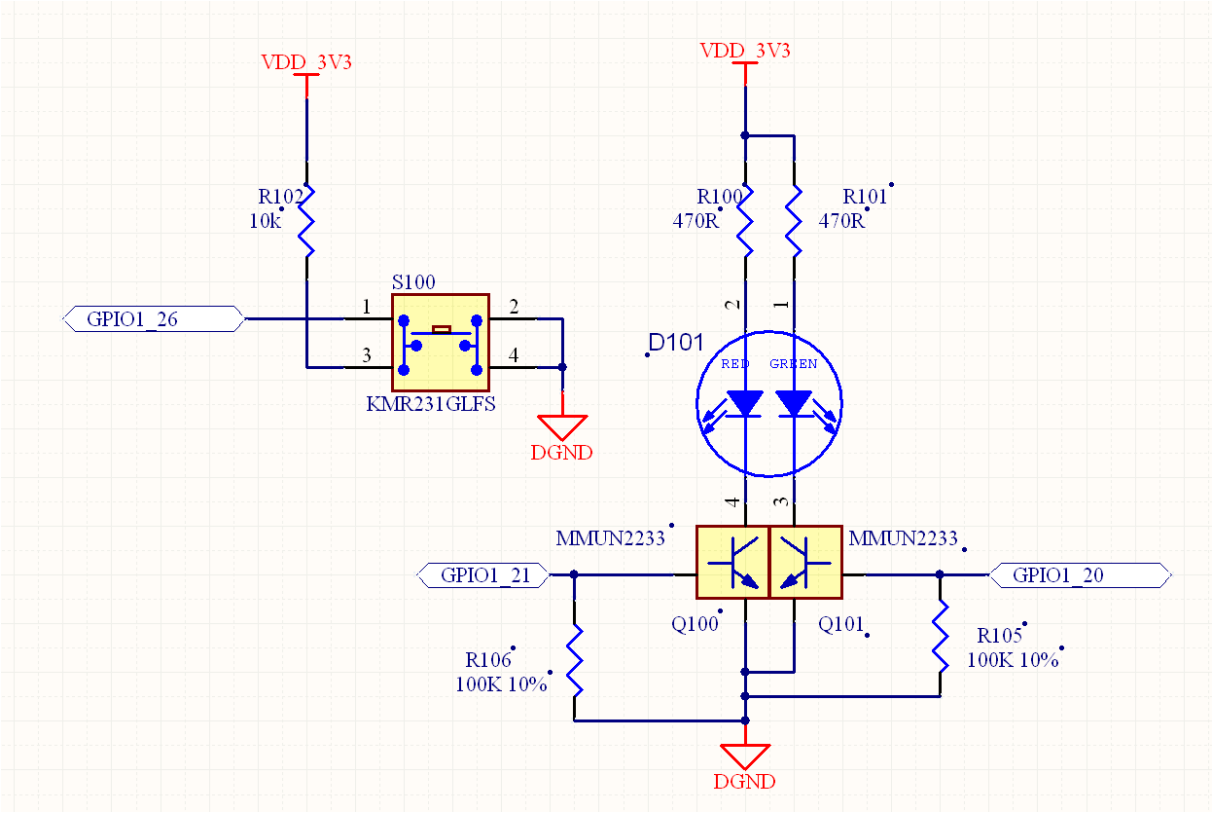


Figure 28 GPIOs example: control circuit to manage LEDs

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 72 | 3V3 | U16 | GPIO1_25 | 7 | IO | No | General purpose input/output |
| 73 | 3V3 | C12 | GPIO3_17 | 7 | IO | No | General purpose input/output |
| 74 | 3V3 | C18 | GPIO0_7 | 7 | IO | No | General purpose input/output |
| 75 | 3V3 | U18 | GPIO1_28 | 7 | IO | No | General purpose input/output |
| 77 | 3V3 | A15 | GPIO0_19 | 7 | IO | No | General purpose input/output |
| 78 | 3V3 | D14 | GPIO0_20 | 7 | IO | No | General purpose input/output |
| 79 | 3V3 | V12 | GPIO2_1 | 7 | IO | No | General purpose input/output |
| 80 | 3V3 | T13 | GPIO2_0 | 7 | IO | No | General purpose input/output |
| 148 | 3V3 | V14 | GPIO1_17 | 7 | IO | No | General purpose input/output |
| 151 | 3V3 | U15 | GPIO1_22 | 7 | IO | No | General purpose input/output |
| 153 | 3V3 | T16 | GPIO1_26 | 7 | IO | No | General purpose input/output |
| 154 | 3V3 | V15 | GPIO1_21 | 7 | IO | No | General purpose input/output |
| 155 | 3V3 | R14 | GPIO1_20 | 7 | IO | No | General purpose input/output |
| 197 | 3V3 | C14 | GPIO3_7 | 7 | IO | No | General purpose input/output |

Table 17 GPIO pins

## 4.15 ADC: General Purpose Analog-to-Digital Converter

The IGEP™ COM AQUILA AM335x includes an analog-to-digital converter subsystem. It's an 8-channel general-purpose converter, with a subsystem to interface with a resistive touchscreen (for a 4-wire, 5-wire and 8-wire resistive panel).

In the next figure is one of the more basic connections to input an analogue voltage signal to the module via an ADC pin.

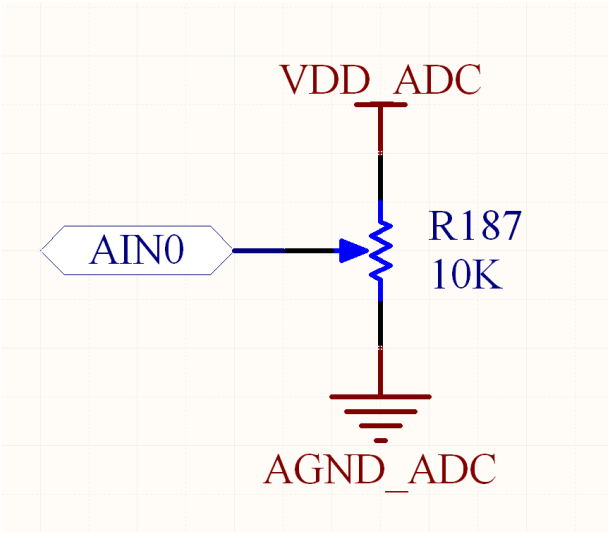


Figure 29 ADC example circuit

| Pin | Volt Level | Dev Pin | Main Function | Main MUX | Type | Fixed Function | Comments |
|---|---|---|---|---|---|---|---|
| 183 | GND | E8 | VSSA_ADC | NA | Power | Yes | Analog Ground for ADCs |
| 184 | 1V8 | D8 | VREFP_ADC | NA | Power | Yes | Supply voltage range for ADCs |
| 185 | ANALOG | B6 | AIN0 | 0 | IN | Yes | General purpose ADC channel 0 |
| 186 | ANALOG | C7 | AIN1 | 0 | IN | Yes | General purpose ADC channel 1 |
| 187 | ANALOG | B7 | AIN2 | 0 | IN | Yes | General purpose ADC channel 2 |
| 188 | ANALOG | A7 | AIN3 | 0 | IN | Yes | General purpose ADC channel 3 |
| 189 | ANALOG | C8 | AIN4 | 0 | IN | Yes | General purpose ADC channel 4 |
| 190 | ANALOG | B8 | AIN5 | 0 | IN | Yes | General purpose ADC channel 5 |
| 191 | ANALOG | A8 | AIN6 | 0 | IN | Yes | General purpose ADC channel 6 |
| 192 | ANALOG | C9 | AIN7 | 0 | IN | Yes | General purpose ADC channel 7 |

Table 18 ADC pins

## 4.16 ENVIRONMENTAL SPECIFICATION

### Temperature Specification

| General _Specification | Operating | Non-operating |
|---|---|---|
| Industrial grade (E2) | -40ºC to +85ºC | -40ºC to +85ºC |

Table 19 Temperature Specification

Standard modules are available for industrial grade temperature range.

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

## 4.17 STANDARDS AND CERTIFICATION

### RoHS

The IGEP™ COM AQUILA AM335x is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

### Assembly Standards

In the assembly of the modules, there are different standards respected.

The components reception is made according tables MIL-STD-105E for sampling and verification guideline of bought products.

In the assembly of SMD components is applied the standard IPC-A-610-E (visual quality acceptability requirements for electronic assemblies).

It is also made an electric test over 100% of modules manufactured.

## 4.18 MTBF

The IGEP™ COM AQUILA AM335x MTBF (hours) : >100,000 hours

The above MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40 °C ambient environment and the system is assumed to have not been burned in.

Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50 °C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40 °C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

## 4.19 MECHANICAL SPECIFICATION

### Module Dimension

- 67,60mm x 26,00mm x 4mm

### Mechanical Drawing

The next figures show the IGEP™ COM AQUILA AM335x modules mechanical dimensions:

- All dimensions are in millimeters.
- 10-layer Printed Circuit Board size is 67.60x26x1mm.
- mounting holes are provided, one on each corner.

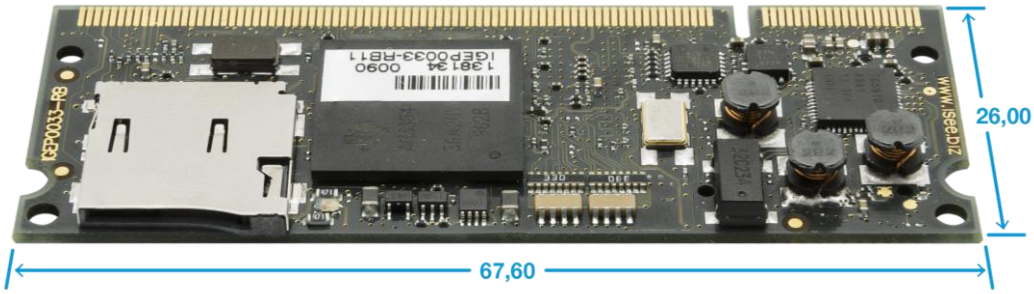


Figure 30 IGEP™ COM AQUILA AM335x Main Outline Dimensions

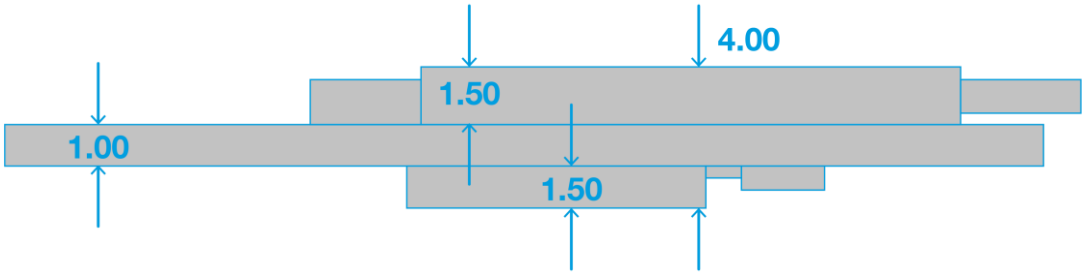


Figure 31 IGEP™ COM AQUILA AM335x Lateral View Widths Dimensions

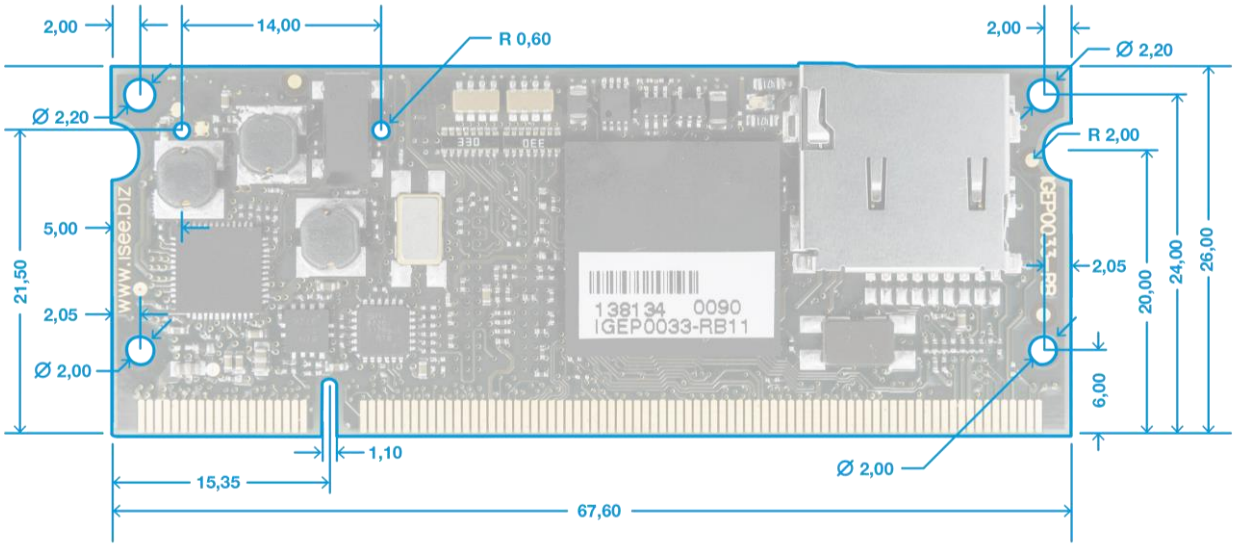


Figure 32 IGEP™ COM AQUILA AM335x TOP side view detailed mechanical

# 5 ON-BOARD INTERFACES

## 5.1 SUMMARY

| Device | Connector | Reference | Comments |
|---|---|---|---|
| microSD | microSD SOCKET | J700 | On-board. Bootable device. |
| LED | - | D100 | Power & GPIO controlled |
| JTAG | 15pin 1mm pitch interface | J800 | Mates with compression connector |
| SODIMM-200 | 200-pin SODIMM interface DDR1 standard 2V5 | K100 | Expand many functionalities from AM335x SITARA processor |

Table 20 Interface Summary

## 5.2 SD: Secure Digital Reader

The on-board micro-SD socket uses the MMC0 controller of the AM335x processor. The module can boot from this SD socket (see 6-SODIMM-200 EXPANSION CONNECTOR INTERFACE chapter for details).

The interface provides the following features:

- Full compliance with MMC4.3 and command/response sets as defined in the SD Memory Card Specifications v2.0
- 4-bit MMC/SD/SDIO Mode 3V3 operation
- Up to 48MHz Data Transfer Rate
- Designed for low power

Compatible with SD/SDHC (up to 32 GB).

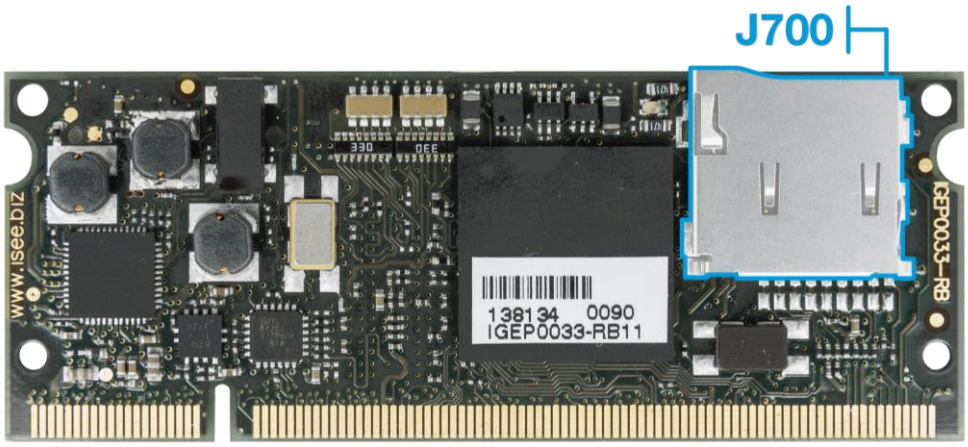


Figure 33 J700 MICRO SD Socket area

## 5.3 LEDs

The IGEP™ COM AQUILA AM335x module provides one bicolor LED indicator on the board. One LED can be controlled by the user.

| Signal Name | LED Color | Description |
|---|---|---|
| 3V3 | Red | 3V3 Internal Power signal |
| GPIO1_23 | Green | GPIO1_23 of AM335x |

Table 21 LEDs pins

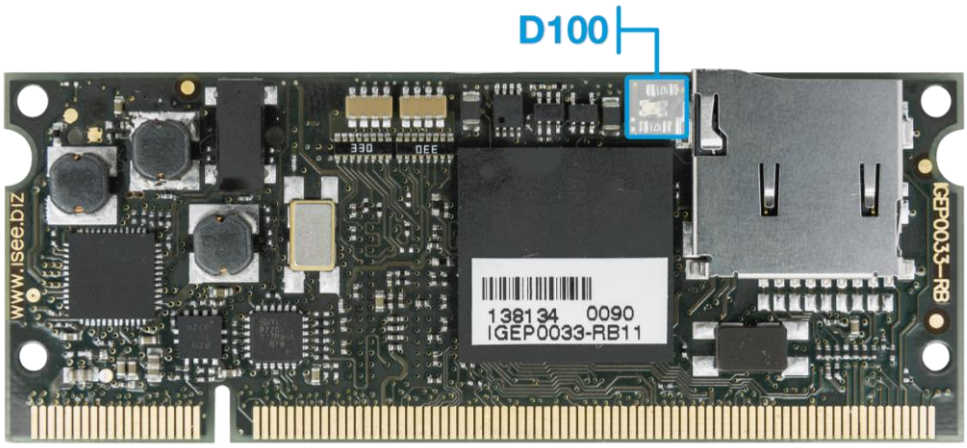


Figure 34 D100 LED area

## 5.4 JTAG

The IGEP™ COM AQUILA AM335x provides a foot print JTAG interface to help you develop your code. The signals can be accessed by means of a compression connector placed on a base board, correctly centered to interface the metal contacts placed on the bottom side of the module.

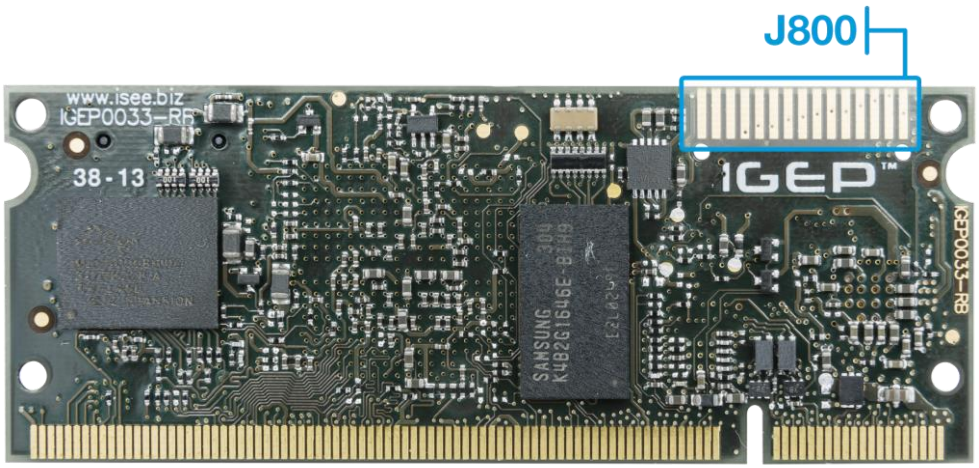


Figure 35 J800 JTAG Interface area

The recommended compression connector part number to be used is FSI-115-03-GS-AD from SAMTEC manufacturer; this is a 15-pin single row 1mm pitch compression connector with 3mm height. The height of this connector has to be in accordance with the height of the used SODIMM 200-pin connector. A double row version can also be used; in this case part number will be FSI-115-03-GD-AD and the second row will not be used so it is better if you leave even pins unconnected.

The next figure shows (a) how to match compression connector with the module board J800, (b) double row compression connector and (c) single row compression connector.

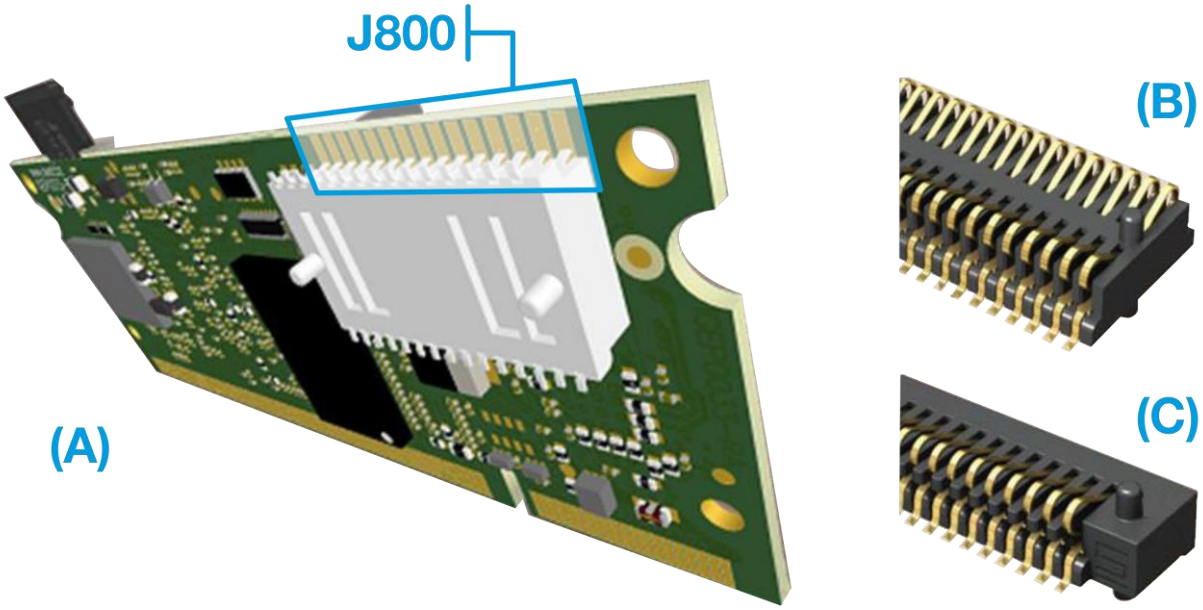


Figure 36 J800 JTAG Interface: compression connector

The next figure shows the pin out schematic and the corresponding metal contacts.

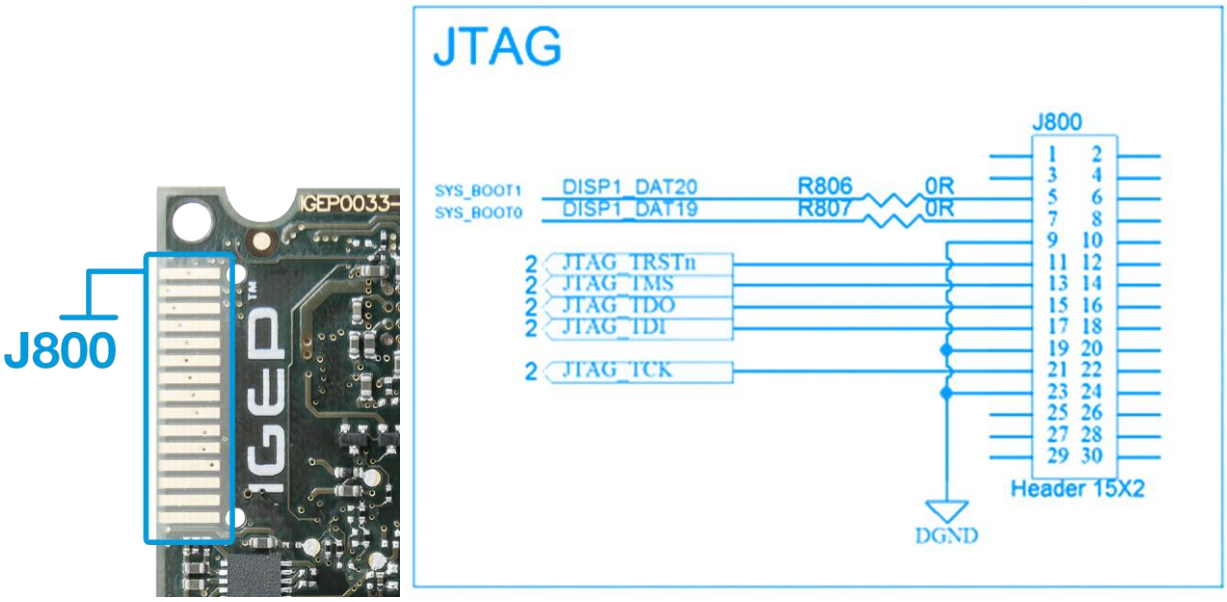


Figure 37 J800 JTAG Interface: foot print and schematic

Note that even pins are left unconnected but the footprint makes possible to use a double row compression connector. The next table details the signals on each pin of J800.

| Signal Name | J800 JTAG PIN | Description |
|---|---|---|
| NC | 1 | Not Connected |
| NC | 3 | Not Connected |
| SYS_BOOT1 | 5 | Bit 1 of the BOOT configuration |
| SYS_BOOT0 | 7 | Bit 0 of the BOOT configuration |
| DGND | 9 | Digital Ground |
| TRSTn | 11 | JTAG Test Reset Input Signal |
| TMS | 13 | JTAG Test Mode Select Input Signal |
| TDO | 15 | JTAG Test Data Output Signal |
| TDI | 17 | JTAG Test Data Input Signal |
| DGND | 19 | Digital Ground |
| TCK | 21 | JTAG Test Clock Input Signal |
| DGND | 23 | Digital Ground |
| NC | 25 | Not Connected |
| NC | 27 | Not Connected |
| NC | 29 | Not Connected |

Table 22 JTAG pins

For additional details about JTAG, please refer to **AM335x ARM Cortex™-A8 Microprocessors (MPUs) Technical Reference Manual**.

# 6 SODIMM-200 EXPANSION CONNECTOR INTERFACE

The IGEP™ COM AQUILA AM335x has 1 SODIMM-200 interface (K100) composed by 200 metal contacts, 100 on TOP side (odd numbers) and 100 on BOTTOM side (even numbers), providing source power and up to 140 signals at 3V3 CMOS to support lots of features of AM335x processor that can be used in your custom baseboard.

The next figure shows the area and pin numbering of the SODIMM-200 interface:

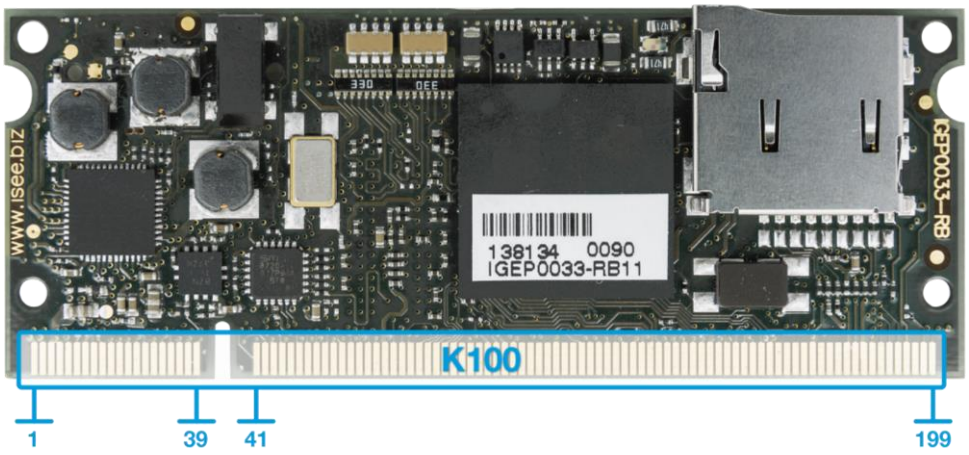


Figure 38 K100 SODIMM-200 interface area (TOP SIDE, odd pin numbering)

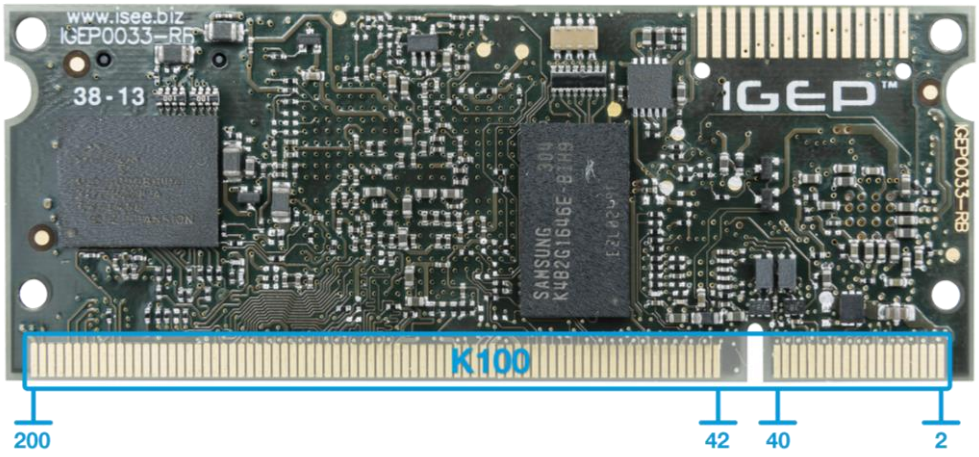


Figure 39 K100 SODIMM-200 interface area (BOTTOM SIDE, even pin numbering)

The IGEP™ COM AQUILA AM335x modules can be inserted like a target through this SODIMM-200 interface to any of the standard SODIMM-200 connectors existing on the market. Some valid references are:

| MANUFACTURER | PART NUMBER | HEIGHT |
|---|---|---|
| TE CONNECTIVITY | 1473005-1 | 5,2mm |
| FOXCONN | AS0A426-E4SN-7F | 4mm |
| TYCO ELECTRONICS | 1565691-1 | 4mm |
| FOXCONN | AS0A426-E2SN-7F | 5,2mm |
| ADMATEC | SODIMM200S92T25 | 9,2mm |

Table 23 Valid SODIMM-200 connectors part numbers

You must consider the SODIMM-200 connector height depending on your base board needs.

## 6.1 PINOUT TABLE OF SODIMM-200 EXPANSION INTERFACE

In this chapter is reflected a table with all the pinout details for the SODIMM-200 expansion interface. In that, are collected all the pins with its main functions. The meanings of each column and the colors used in rows are next.

| COLUMN | INFORMATION PROVIDED | |
|---|---|---|
| PIN | Indicates the pin number of the SODIMM-200 interface. | |
| VOLTAGE LEVEL | Signal level voltage. | |
| | 5V | 5V signal |
| | 3V3 | 3,3 V signal |
| | 1V8 | 1,8 V signal |
| | VBAT | Battery power |
| | DIF | Differential pair signal |
| | ANALOG | Analog signal |
| | GND | Digital ground |
| | AGND | Analog ground |
| | NC | No connected. This pin should be floating |
| DEV PIN | Internal main device pin number related to the AM335x processor. | |
| MAIN FUNCTION | Main or suggested function. | |
| MAIN MUX | Mode number for the main function. | |
| TYPE | Indicates pin type. | |
| | POWER | Power signal |
| | IN | CMOS input pin |
| | OUT | CMOS output pin |
| | IO | CMOS input and output pin |
| | ETH | Ethernet physical pin |
| | USB | USB line |
| | NC | No connected. This pin should be floating |
| | VK | Power supply from battery |
| FIXED FUNCTION | Indicates if the pin function is configurable or not. | |
| | YES | Pin functionality or mux configuration can't be changed |
| | NO | Pin can be configured as another peripheral (mux configurable). See MUX chapter for more information. |
| COMMENTS | Clarifications for the related SODIMM-200 pin. See Device chapter for more information. | |

| ROW COLOR | INFORMATION PROVIDED | |
|---|---|---|
| GREY | NC | No connected |
| BLUE | VIN | Input power |
| VIOLET | VOUT | Output power |
| CINNAMON | RTC | RTC battery positive signal |
| LIGHT GREEN | DGND | Digital ground |
| DARK GREEN | AGND | Analog ground |
| YELLOW | ETH | Ethernet group |
| LIGHT BROWN | USB0 | USB OTG |
| DARK BROWN | USB1 | USB HOST |
| RED | | Control and Boot signals |
| WHITE | | Low level peripherals |

| SODIM M-200 | | INTERNAL DEVICE | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|
| Pin | Voltage level | Dev Pin | Main function | Main MUX | Type | Fixed Function | |
| 5V INPUT POWER | | | | | | | |
| 1 | 5V | NC | VIN | NA | POWER | Yes | Pins used to power up the module<br>Source voltage should be between 4V-5.5V |
| 2 | 5V | NC | VIN | NA | POWER | Yes | |
| 3 | 5V | NC | VIN | NA | POWER | Yes | |
| 4 | 5V | NC | VIN | NA | POWER | Yes | |
| 3V3 OUTPUT POWER | | | | | | | |
| 5 | 3V3 | NC | VOUT | NA | POWER | Yes | Pins 5,6,7,9,10,11 and 12 used as external 3V3@1A source voltage for a base board |
| 6 | 3V3 | NC | VOUT | NA | POWER | Yes | |
| 7 | 3V3 | NC | VOUT | NA | POWER | Yes | |
| BOOT MODE | | | | | | | |
| 8 | 3V3 | T1 | #SYS_BOOT4 | 0 | IN | Yes | SYS_BOOT4 signal inverted. Sequence should be:<br>NC: UART0→ SPI0→ XIP → MMC0<br>Tied to GND: NAND→ NANDI2C→ MMC0 → UART0 |
| 3V3 OUTPUT POWER | | | | | | | |
| 9 | 3V3 | NC | VOUT | NA | POWER | Yes | Pins 5,6,7,9,10,11 and 12 used as external 3V3@1A source voltage for a base board |
| 10 | 3V3 | NC | VOUT | NA | POWER | Yes | |
| 11 | 3V3 | NC | VOUT | NA | POWER | Yes | |
| 12 | 3V3 | NC | VOUT | NA | POWER | Yes | |
| CONTROL SIGNALS | | | | | | | |
| 13 | VBAT | NC | RTC_BATTERY | NA | POWER | Yes | RTC battery positive pin. Battery or capacitor limit voltage should be:<br>2V52; 3V; 3V15 and VIN |
| 14 | 5V | NC | #PWRKILL | NA | IN | Yes | Tied to GND to cut off power sources from PMIC |
| 15 | 3V3 | B14 | #RESET_OUT | 7 | OUT | Yes | This pins is used as external reset source for a base board<br>Active Low |
| 16 | 3V3 | B15 | PORZ | 0 | IO | Yes | Power ON Reset. Active Low. |
| 17 | 3V3 | A10 | WARMRSTn | 0 | IO | Yes | Warm Reset. Active Low. |
| 18 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| ETHERNET | | | | | | | |
| 19 | DIF | NC | ETN_TXM | NA | ETH | Yes | Analog Transmit Data Negative. Differential output to magnetics |
| 20 | 3V3 | NC | #ETN_LED2 | NA | OUT | Yes | Active Low. LED2 Yellow means 100Mbps speed.<br>Inactive if 10Mbps.<br>Line isolated through a driver. |
| 21 | DIF | NC | ETN_TXP | NA | ETH | Yes | Analog Transmit Data Positive. Differential output to magnetics |
| 22 | 3V3 | NC | ETN_3V3 | NA | POWER | Yes | 3V3 to magnetics |
| 23 | DIF | NC | ETN_RXM | NA | ETH | Yes | Analog Receive Data Negative. Differential output to magnetics |
| 24 | 3V3 | NC | #ETN_LED1 | NA | OUT | Yes | Active Low. LED1 Green indicates valid link and blinks when there is activity.<br>Line isolated through a driver |
| 25 | DIF | NC | ETN_RXP | NA | ETH | Yes | Analog Receive Data Poitive. Differential output to magnetics |
| 26 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| USB HOST | | | | | | | |
| 27 | 3V3 | F15 | USB1_DRVVBUS | 0 | OUT | Yes | Active High. Enables external VBUS power supply |
| 28 | 3V3 | R13 | GPIO1_16 | 7 | IN | No | #USB1_OC: Active Low. Over current indication to module. It could be another GPIO from uP. |
| 29 | DIF | R18 | USB1_DM | 0 | USB | Yes | Analog D- data pin of the USB cable |
| 30 | 5V | T18 | USB1_VBUS | 0 | POWER | Yes | VBUS pin of the USB cable. |
| 31 | DIF | R17 | USB1_DP | 0 | USB | Yes | Analog D+ data pin of the USB cable |
| 32 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |

| SODIM M-200 | | INTERNAL DEVICE | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|
| Pin | Voltage level | Dev Pin | Main function | Main MUX | Type | Fixed function | |
| USB OTG | | | | | | | |
| 33 | ANALOG | P16 | USB0_ID | 0 | USB | Yes | ID pin of the USB cable. A-device is grounded; B-device is floating |
| 34 | 3V3 | F16 | USB0_DRVVBUS | 0 | OUT | Yes | Active High. Enables external VBUS power supply |
| 35 | DIF | N18 | USB0_DM | 0 | USB | Yes | Analog D- data pin of the USB cable |
| 36 | 3V3 | V17 | GPIO1_27 | 7 | IN | No | #USB0_OC: Active Low. Over current indication to module. It could be another GPIO from uP. |
| 37 | DIF | N17 | USB0_DP | 0 | USB | Yes | Analog D+ data pin of the USB cable |
| 38 | 5V | P15 | USB0_VBUS | 0 | POWER | Yes | VBUS pin of the USB cable. |
| 39 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| I2C INTERFACE | | | | | | | |
| 40 | 3V3 | C17 | I2C0_SDA | 0 | IO | Yes | I2C0 bus data. 0x2D is used. by IGEP COM Aquila This signal has a 5K PU resistor. |
| 41 | 3V3 | C16 | I2C0_SCL | 0 | IO | Yes | I2C0 bus clock. This signal has a 5K PU resistor. |
| PWM | | | | | | | |
| 42 | NC | NC | No connected | NA | NC | NA | No connected |
| OWIRE: ONE WIRE INTERFACE | | | | | | | |
| 43 | NC | NC | No connected | NA | NC | NA | No connected |
| CSPI: SERIAL PERIPHERAL INTERFACE | | | | | | | |
| 44 | 3V3 | A16 | SPI0_CS0 | 0 | OUT | No | SPI0 Slave chip select 0 signal |
| 45 | 3V3 | C15 | SPI0_CS1 | 0 | OUT | No | SPI0 Slave chip select 1 signal |
| 46 | 3V3 | B17 | SPI0_D0 | 0 | OUT | No | SPI0 Master Output-Slave Input (MOSI) |
| 47 | 3V3 | B16 | SPI0_D1 | 0 | IN | No | SPI0 Master Input-Slave Output (MISO) |
| 48 | 3V3 | A17 | SPI0_SCLK | 0 | OUT | No | SPI0 Clock |
| 49 | NC | NC | No connected | NA | NC | NA | No connected |
| 50 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| uSD1: SECURE DIGITAL INTERFACE 1 | | | | | | | |
| 51 | 3V3 | B13 | MMC1_SDCD | 4 | IN | No | SD Card Detect for MMC1. There are no components between this pin and AM335x ball |
| 52 | 3V3 | K18 | MMC1_DAT0 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 0. There are no components between this pin and AM335x ball |
| 53 | 3V3 | L18 | MMC1_DAT1 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus Bus 1. There are no components between this pin and AM335x ball |
| 54 | 3V3 | L17 | MMC1_DAT2 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 2. There are no components between this pin and AM335x ball |
| 55 | 3V3 | L16 | MMC1_DAT3 | 4 | IO | No | MMC/SD/SDIO 1 Data Bus 3. There are no components between this pin and AM335x ball |
| 56 | 3V3 | V9 | MMC1_CMD | 2 | IO | No | MMC/SD/SDIO 1 Command. There are no components between this pin and AM335x ball |
| 57 | 3V3 | U9 | MMC1_CLK | 2 | IO | No | MMC/SD/SDIO 1 Clock There are no components between this pin and AM335x ball |
| 58 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| 1ST UART | | | | | | | |
| 59 | 3V3 | E16 | UART0_TXD | 0 | OUT | No | Debug UART0 Transmit Data Output |
| 60 | 3V3 | E15 | UART0_RXD | 0 | IN | No | Debug UART0 Receive Data Intput |
| 61 | 3V3 | E18 | UART0_CTSn | 0 | IN | No | UART0 CTSn Input |
| 62 | 3V3 | E17 | UART0_RTSn | 0 | OUT | No | UART0 RTSn Output |
| 2ND UART | | | | | | | |
| 63 | 3V3 | D15 | UART1_TXD | 0 | OUT | No | UART1 Transmit Data Output |
| 64 | 3V3 | D16 | UART1_RXD | 0 | IN | No | UART1 Receive Data Intput |
| 65 | 3V3 | D18 | UART1_CTSn | 0 | IN | No | UART1 CTSn Input |
| 66 | 3V3 | D17 | UART1_RTSn | 0 | OUT | No | UART1 RTSn Output |

| SODIM M-200 | | INTERNAL DEVICE | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|
| Pin | Voltage level | Dev Pin | Main function | Main MUX | Type | Fixed function | |
| 3RD UART | | | | | | | |
| 67 | 3V3 | J17 | UART5_TXD | 3 | OUT | No | UART5 Transmit Data Output |
| 68 | 3V3 | H16 | UART5_RXD | 3 | IN | No | UART5 Receive Data Intput |
| 69 | NC | NC | No connected | NA | NC | NA | No connected |
| 70 | NC | NC | No connected | NA | NC | NA | No connected |
| 71 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| GPIO / CAN | | | | | | | |
| 72 | 3V3 | U16 | GPIO1_25 | 7 | IO | No | General purpose input/output |
| 73 | 3V3 | C12 | GPIO3_17 | 7 | IO | No | General purpose input/output |
| 74 | 3V3 | C18 | GPIO0_7 | 7 | IO | No | General purpose input/output |
| 75 | 3V3 | U18 | GPIO1_28 | 7 | IO | No | General purpose input/output |
| 76 | 3V3 | J18 | DCAN0_TX | 1 | O | No | CAN0 Transmission line |
| 77 | 3V3 | A15 | GPIO0_19 | 7 | IO | No | General purpose input/output |
| 78 | 3V3 | D14 | GPIO0_20 | 7 | IO | No | General purpose input/output |
| 79 | 3V3 | V12 | GPIO2_1 | 7 | IO | No | General purpose input/output |
| 80 | 3V3 | T13 | GPIO2_0 | 7 | IO | No | General purpose input/output |
| 81 | 3V3 | K15 | DCAN0_RX | 1 | I | No | CAN0 Reception line |
| 82 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| SSI 1: SERIAL AUDIO PORT 1 | | | | | | | |
| 83 | 3V3 | D12 | MCASP0_AXR0 | 0 | IO | No | McASP0 Serial Data (IN/OUT) 0 |
| 84 | 3V3 | D13 | MCASP0_AXR1 | 0 | IO | No | McASP0 Serial Data (IN/OUT) 1 |
| 85 | 3V3 | A14 | MCASP0_AHCLKX | 0 | IO | No | McASP0 Transmit Master Clock |
| 86 | 3V3 | B12 | MCASP0_ACLKR | 0 | IO | No | McASP0 Receive Bit Clock |
| 87 | 3V3 | C13 | MCASP0_FSR | 0 | IO | No | McASP0 Receive Frame Sync |
| 88 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| SSI 2: SERIAL AUDIO PORT 2 | | | | | | | |
| 89 | NC | NC | No connected | NA | NC | NA | No connected |
| 90 | NC | NC | No connected | NA | NC | NA | No connected |
| 91 | NC | NC | No connected | NA | NC | NA | No connected |
| 92 | NC | NC | No connected | NA | NC | NA | No connected |
| 93 | NC | NC | No connected | NA | NC | NA | No connected |
| 94 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| uSD2: SECURE DIGITAL INTERFACE 2 | | | | | | | |
| 95 | NC | NC | No connected | NA | NC | NA | No connected |
| 96 | NC | NC | No connected | NA | NC | NA | No connected |
| 97 | NC | NC | No connected | NA | NC | NA | No connected |
| 98 | NC | NC | No connected | NA | NC | NA | No connected |
| 99 | NC | NC | No connected | NA | NC | NA | No connected |
| 100 | NC | NC | No connected | NA | NC | NA | No connected |
| 101 | NC | NC | No connected | NA | NC | NA | No connected |
| 102 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |

| SODIM M-200 | | INTERNAL DEVICE | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|
| Pin | Voltage level | Dev Pin | Main function | Main MUX | Type | Fixed function | |
| CMOS SENSOR INTERFACE | | | | | | | |
| 103 | NC | NC | No connected | NA | NC | NA | No connected |
| 104 | NC | NC | No connected | NA | NC | NA | No connected |
| 105 | NC | NC | No connected | NA | NC | NA | No connected |
| 106 | NC | NC | No connected | NA | NC | NA | No connected |
| 107 | NC | NC | No connected | NA | NC | NA | No connected |
| 108 | NC | NC | No connected | NA | NC | NA | No connected |
| 109 | NC | NC | No connected | NA | NC | NA | No connected |
| 110 | NC | NC | No connected | NA | NC | NA | No connected |
| 111 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| 112 | NC | NC | No connected | NA | NC | NA | No connected |
| 113 | NC | NC | No connected | NA | NC | NA | No connected |
| 114 | NC | NC | No connected | NA | NC | NA | No connected |
| 115 | NC | NC | No connected | NA | NC | NA | No connected |
| 116 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| LCD CONTROLLER | | | | | | | |
| 117 | 3V3 | U10 | LCD_DATA23 | 1 | O | No | LCD data bus |
| 118 | 3V3 | U12 | LCD_DATA20 | 1 | O | No | LCD data bus |
| 119 | 3V3 | V13 | LCD_DATA17 | 1 | O | No | LCD data bus |
| 120 | 3V3 | U4 | LCD_DATA11 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 121 | 3V3 | V2 | LCD_DATA12 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 122 | 3V3 | V3 | LCD_DATA13 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 123 | 3V3 | V4 | LCD_DATA14 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 124 | 3V3 | T5 | LCD_DATA15 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 125 | 3V3 | T10 | LCD_DATA22 | 1 | O | No | LCD data bus |
| 126 | 3V3 | T12 | LCD_DATA19 | 1 | O | No | LCD data bus |
| 127 | 3V3 | T2 | LCD_DATA5 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 128 | 3V3 | T3 | LCD_DATA6 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 129 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| 130 | 3V3 | T4 | LCD_DATA7 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 131 | 3V3 | U1 | LCD_DATA8 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 132 | 3V3 | U2 | LCD_DATA9 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 133 | 3V3 | U3 | LCD_DATA10 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 134 | 3V3 | T11 | LCD_DATA21 | 1 | O | No | LCD data bus |
| 135 | 3V3 | R12 | LCD_DATA18 | 1 | O | No | LCD data bus |
| 136 | 3V3 | U13 | LCD_DATA16 | 1 | O | No | LCD data bus |
| 137 | 3V3 | R1 | LCD_DATA0 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 138 | 3V3 | R2 | LCD_DATA1 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 139 | 3V3 | R3 | LCD_DATA2 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 140 | 3V3 | R4 | LCD_DATA3 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 141 | 3V3 | T1 | LCD_DATA4 | 0 | IO | No | LCD data bus. High value PU/PD used for SYSBOOT |
| 142 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |

| SODIM M-200 | | INTERNAL DEVICE | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|
| Pin | Voltage level | Dev Pin | Main function | Main MUX | Type | Fixed function | |
| 143 | 3V3 | R5 | LCD_HSYNC | 0 | OUT | No | LCD Horizontal Sync |
| 144 | 3V3 | U5 | LCD_VSYNC | 0 | OUT | No | LCD Vertical Sync |
| 145 | 3V3 | R6 | LCD_AC_BIAS_EN | 0 | OUT | No | LCD AC bias enable chip select |
| 146 | 3V3 | V5 | LCD_PCLK | 0 | OUT | No | LCD pixel clock |
| 147 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| OTHER SIGNALS (ADCs, GPIOs, PWM) | | | | | | | |
| 148 | 3V3 | V14 | GPIO1_17 | 7 | IO | No | General purpose input/output |
| 149 | 3V3 | U14 | EHRPWM1A | 6 | OUT | No | eHRPWM1 A output. |
| 150 | 3V3 | T14 | EHRPWM1B | 6 | OUT | No | eHRPWM1 B output. |
| 151 | 3V3 | U15 | GPIO1_22 | 7 | IO | No | General purpose input/output |
| 152 | NC | NC | No connected | NA | NC | NA | No connected |
| 153 | 3V3 | T16 | GPIO1_26 | 7 | IO | No | General purpose input/output |
| 154 | 3V3 | V15 | GPIO1_21 | 7 | IO | No | General purpose input/output |
| 155 | 3V3 | R14 | GPIO1_20 | 7 | IO | No | General purpose input/output |
| 156 | NC | NC | No connected | NA | NC | NA | No connected |
| 157 | NC | NC | No connected | NA | NC | NA | No connected |
| 158 | 3V3 | V16 | McASP0_ACLKX | 6 | IO | No | McASP0 Transmit Bit Clock |
| 159 | NC | NC | No connected | NA | NC | NA | No connected |
| 160 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| 161 | NC | NC | No connected | NA | NC | NA | No connected |
| 162 | NC | NC | No connected | NA | NC | NA | No connected |
| 163 | NC | NC | No connected | NA | NC | NA | No connected |
| 164 | NC | NC | No connected | NA | NC | NA | No connected |
| 165 | NC | NC | No connected | NA | NC | NA | No connected |
| 166 | NC | NC | No connected | NA | NC | NA | No connected |
| 167 | NC | NC | No connected | NA | NC | NA | No connected |
| 168 | NC | NC | No connected | NA | NC | NA | No connected |
| 169 | NC | NC | No connected | NA | NC | NA | No connected |
| 170 | NC | NC | No connected | NA | NC | NA | No connected |
| 171 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |
| 172 | NC | NC | No connected | NA | NC | NA | No connected |
| 173 | NC | NC | No connected | NA | NC | NA | No connected |
| 174 | NC | NC | No connected | NA | NC | NA | No connected |
| 175 | NC | NC | No connected | NA | NC | NA | No connected |
| 176 | NC | NC | No connected | NA | NC | NA | No connected |
| 177 | NC | NC | No connected | NA | NC | NA | No connected |
| 178 | NC | NC | No connected | NA | NC | NA | No connected |
| 179 | NC | NC | No connected | NA | NC | NA | No connected |
| 180 | NC | NC | No connected | NA | NC | NA | No connected |
| 181 | NC | NC | No connected | NA | NC | NA | No connected |
| 182 | NC | NC | No connected | NA | NC | NA | No connected |
| 183 | AGND | E8 | VSSA_ADC | NA | POWER | Yes | Analog Ground for ADCs |

| SODIM M-200 | | INTERNAL DEVICE | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|
| Pin | Voltage level | Dev Pin | Main function | Main MUX | Type | Fixed function | |
| 184 | 1V8 | D8 | VREFP_ADC | NA | POWER | Yes | Supply voltage range for ADCs |
| 185 | ANALOG | B6 | AIN0 | 0 | IN | Yes | General purpose ADC channel 0 |
| 186 | ANALOG | C7 | AIN1 | 0 | IN | Yes | General purpose ADC channel 1 |
| 187 | ANALOG | B7 | AIN2 | 0 | IN | Yes | General purpose ADC channel 2 |
| 188 | ANALOG | A7 | AIN3 | 0 | IN | Yes | General purpose ADC channel 3 |
| 189 | ANALOG | C8 | AIN4 | 0 | IN | Yes | General purpose ADC channel 4 |
| 190 | ANALOG | B8 | AIN5 | 0 | IN | Yes | General purpose ADC channel 5 |
| 191 | ANALOG | A8 | AIN6 | 0 | IN | Yes | General purpose ADC channel 6 |
| 192 | ANALOG | C9 | AIN7 | 0 | IN | Yes | General purpose ADC channel 7 |
| 193 | 1V8 | C5 | EXT_WAKEUP | 0 | IN | Yes | EXT_WAKEUP input |
| 194 | NC | NC | No connected | NA | NC | NA | No connected |
| 195 | NC | NC | No connected | NA | NC | NA | No connected |
| 196 | NC | NC | No connected | NA | NC | NA | No connected |
| 197 | 3V3 | C14 | gpio3_7 | 7 | IO | No | General purpose input/output |
| 198 | NC | NC | No connected | NA | NC | NA | No connected |
| 199 | NC | NC | No connected | NA | NC | NA | No connected |
| 200 | GND | NC | DGND | NA | POWER | Yes | Digital Ground |

Table 24 K100 SODIMM-200 pin out description

# 7 ELECTRICAL CHARACTERISTICS

| Electrical parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **5V INPUT POWER SUPPLY** | | | | |
| IGEP™ COM AQUILA AM335x DC INPUT POWER SUPPLY | 3.8 | 5 | 5.5 | V |
| IGEP™ COM AQUILA AM335x DC INPUT SUPPLY Current (1) | 80 | 400 | 550 | mA |
| **5V type pins** | | | | |
| 5V type pins Input Voltage DC | 4 | 5 | 5.5 | V |
| **3V3 OUTPUT POWER SUPPLY** | | | | |
| IGEP™ COM AQUILA AM335x DC OUTPUT POWER SUPPLY | 3.1 | 3.3 | 3.5 | V |
| IGEP™ COM AQUILA AM335x DC OUTPUT SUPPLY Current | 0 | | 1000 | mA |
| **JTAG, IN, OUT and IO LVCMOS type pins** (2) | | | | |
| Input/output High-Level DC voltage | 2.85 | 3.3 | 3.4 | V |
| Input/output Low-Level DC voltage | -0.1 | 0 | 0.45 | V |
| Output drive current | 0 | 0.5 | 1 | mA |
| **ETH type pins** | | | | |
| Input/output High-Level DC voltage | 2.9 | 3.3 | 3.4 | V |
| Input/output Low-Level DC voltage | -0.1 | 0 | 0.5 | V |
| Output drive current | 0 | 1 | 2 | mA |
| **USB type pins** | | | | |
| Input/output High-Level DC voltage | 2.8 | 3.3 | 3.3 | V |
| Input/output Low-Level DC voltage | -0.1 | 0 | 0.4 | V |
| Output drive current | 0 | 1 | 2 | mA |
| **RTC_BATTERY type pins** | | | | |
| Input DC voltage | 0 | 3.1 | 5.5 | V |
| **ADC type pins** | | | | |
| Input DC voltage | 0 | | 1.8 | V |
| Drive current | 0 | | 10 | mA |

Table 25 Electrical characteristics

*(1) Current measured with default delivered software. Be aware that different software configurations could drastically modify current consumption.*

*(2) The electrical specification depends on the configured mode. For accurate information of each pin, revise AM335x Applications Processor official document from Texas Instruments official site [http://focus.ti.com](http://focus.ti.com).*

**IGEP™ COM AQUILA AM335x** MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED. **WARRANTY LOST** IF IMPROPER USE OF THE MODULE IS FOUND

# 8 LIST OF TABLES



# 9 LIST OF FIGURES

# 10 CHANGE HISTORY

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2013/Jan/28 | • Preliminary version (IGEP0033-RAxx) |
| 2.0 | 2013/Jul/12 | • Second version for revised pcb (IGEP0033-RBxx)<br>○ CYGNUS references deleted<br>○ AQUILA references updated to AQUILA AM335x<br>○ Document code/revision/date added to cover<br>○ Footer added (page number and document/revision/date)<br>○ Updated order information for IGEP0033-RB1x, IGEP0033-RB2x, IGEP0033-RB3x and IGEP0033-RB4x<br>○ Generic Bloc Diagram for AM335x<br>○ Updated pin out tables from RA<br>▪ change: swapped 28 pin <-> 34 pin<br>▪ change: 184 pin VREFP_ADC output voltatge (1v8)<br>○ Minor changes |
| 2.1 | 2013/Jul/22 | • Quality revision<br>○ Added TI AM335x Family Features figure<br>○ Updated Bloc Diagram (2 Ethernet peripherals) |
| 2.2 | 2013/Set/30 | • Quality revision<br>○ Change code IGEP0033-RB1x for AM3354<br>• Change code IGEP0033-RB2x for AM3352 |
| 3.0 | 2016/Jun/27 | • Quality revision<br>○ Additions to USER INFORMATION chapter<br>○ Additions to INTRODUCTION chapter<br>○ Updated description in Ordering Information table<br>○ Updated Features table<br>○ Added informative chapter about the AM335x processor variants<br>○ Added informative chapter about the AM335x processor<br>○ Updated Block Diagram<br>○ Updated technical information<br>○ Updated ON-BOARD INTERFACES chapter<br>○ Updated SODIMM EXPANSION CONNECTOR INTERFACE chapter<br>○ Changed pinout table of SODIMM-200 connector<br>○ Updated electrical characteristics table |

Please check for a newer revision of this manual at ISEE 2007 SL web site http://www.isee.biz